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A Reduced Latency Architecture for Obtaining High System Performance

Kareemullah Shaik, Mohammad Mohiddin, Md. Zabirullah

***Abstract*— Microprocessor performance has improved rapidly these years. In contrast, memory latencies and bandwidths have improved little. The result is that the memory access time has been a bottleneck which limits the system performance. As the speed of fetching data from memories is not able to match up with speed of processors. So there is the need for a fast memory controller. The responsibility of the controller is to match the speeds of the processor on one side and memory on the other so that the communication can take place seamlessly. Here we have built a memory controller which is specifically targeted for SDRAM. Certain features were included in the design which could increase the overall efficiency of the controller, such as, searching the internal memory of the controller for the requested data for the most recently used data, instead of going to the Memory to fetch it.**

The memory controller is designed which compatible with Advanced High-performance Bus (AHB) which is a new generation of AMBA bus. The AHB is for high-performance, high clock frequency system modules. The AHB acts as the high-performance system backbone bus. AHB supports the efficient connection of processors, on-chip memories and off-chip external memory interfaces with low-power peripherals.

Keywords: SDRAM, Memory controller, AMBA, FPGA, Xilinx, Modelsim.

I. INTRODUCTION

In order to enhance overall performance, SDRAMs offer features including multiple internal banks, burst mode access, and pipelining of operation executions. Accessing one bank while precharging other banks is enabled by the feature of multiple internal banks. By using burst mode access in a memory row, current SDRAM architectures can reduce the overhead due to access latency. The pipelining feature permits the controller to send commands to other banks while data is delivered to or from the currently active bank, so that idle time during access latency can be eliminated. This technique is also called interleaving.

The design two way cable networked SoC, that is SDRAM controller connected by AMBA The AMBA AHB is for high-performance, high clock frequency system modules. The AHB acts as the high-performance system backbone bus. AHB supports the efficient connection of processors, on-chip memories and off-chip external memory interfaces with low-power peripherals. It has their own bandwidth requirements and responding speed requirements for SDRAM. By analyzing the multiple accesses from the modules and the SDRAM Specifications such as its accessing delay, we take both side 1 and side 2 into consideration respectively. On side 1, we use bank closing control. On side 2, the controller employs two data write FIFO to reduce the data access awaiting time, and uses 2 read FIFO to decrease the CAS delay time when reading data from SDRAM.

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II. AMBA

The Advanced Microcontroller Bus Architecture (AMBA) specification defines an on chip communications standard for designing high-performance embedded microcontrollers. AMBA (Advanced Microcontroller Bus Architecture), is a bus standard devised by ARM with aim to support efficient on-chip communications among ARM processor cores.

Nowadays, AMBA is one of the leading on-chip busing systems used in high performance SoC design. AMBA is hierarchically organized into two bus segments, system- and peripheral-bus, mutually connected via bridge that FIFO data operations between them. Standard bus protocols for connecting on-chip.

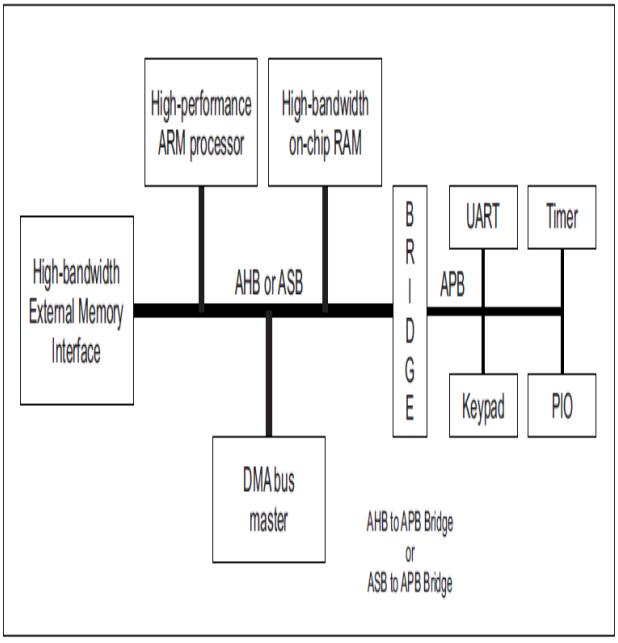

Fig.2.1. A Typical AMBA System

A. Advanced High-performance Bus (AHB)

AHB is a new generation of AMBA bus which is intended to address the requirements of high-performance synthesizable designs. It is a high-performance system bus that supports multiple bus masters and provides high-bandwidth operation. AHB is for high clock frequency system modules.

It acts as the high-performance system backbone bus. AHB supports the efficient connection of processors, on-chip memories and off-chip external memory interfaces with low-power peripherals. Bridging between this higher level of bus and the current ASB/APB can be done efficiently to ensure that any existing designs can be easily integrated. An AMBA AHB design may contain one or more bus masters, typically a system would contain at least the processor and test interface.

B. Advanced System Bus (ASB)

The Advanced System Bus (ASB) specification defines a high-performance bus that can be used in the design of high performance 16 and 32-bit embedded microcontrollers. AMBA ASB supports the efficient connection of processors, on-chip memories and off chip external memory interfaces with low-power peripherals. An AMBA-ASB based microcontroller typically consists of a high-performance system backbone bus, able to sustain the external memory bandwidth, on which the CPU and other Direct Memory Access (DMA) devices reside.

C. *Advanced Peripheral Bus (APB)*

The Advanced Peripheral Bus (APB) is part of the Advanced Microcontroller Bus Architecture (AMBA) hierarchy of buses and is optimized for minimal power consumption and reduced interface complexity. The AMBA APB should be used to interface to any peripherals which are low bandwidth and do not require the high performance of a pipelined bus interface. The latest revision of the APB ensures that all signal transitions are only related to the rising edge of the clock.

III. SDRAM

Random access memory (RAM) is a form of computer data storage. A random access device allows stored data to be accessed in very nearly the same amount of time for any storage location, so data can be accessed quickly in any random order. In contrast, other data storage media such as hard, CDs, DVDs and magnetic tape read and write.

A. SRAM

Static random-access memory (SRAM) is a type of semiconductor memory that uses bistable latching circuitry to store each bit. SRAM exhibits data remanence, [1] but is still volatile in the conventional sense that data is eventually lost when the memory is not powered. Each bit in an SRAM is stored on four transistors (M1, M2, M3, and M4) that form two cross-coupled inverters.

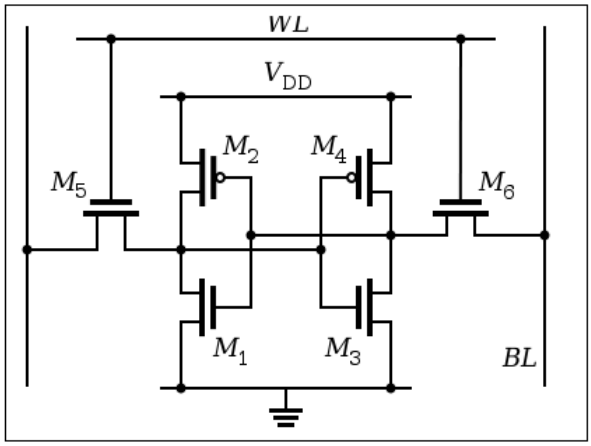

Fig.3.1. A Basic SRAM cell.

B. DRAM

Dynamic random-access memory (DRAM) is a type of random-access memory that stores each bit of data in a separate capacitor within an integrated. The capacitor can be either charged or discharged; these two states are taken to represent the two values of a bit, conventionally called 0 and 1. Since capacitors leak charge, the information eventually fades unless the capacitor charge is refreshed periodically. Because of this refresh requirement, it is a dynamic memory as opposed to SRAM and other static memory. Unlike flash memory, DRAM is volatile.

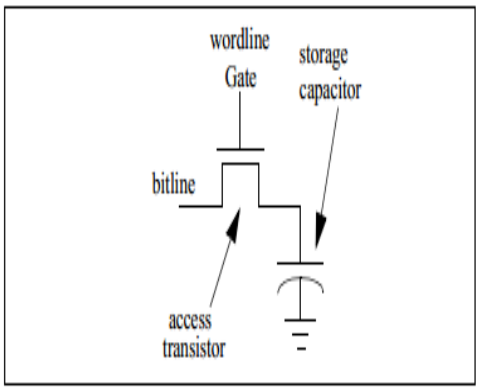

Fig.3.2. A Basic DRAM Cell

C. SDRAM

Synchronous dynamic random access memory (SDRAM) is DRAM that is synchronized with the system bus. Classic DRAM has an asynchronous interface, which means that it responds as quickly as possible to changes in control inputs. SDRAM has a synchronous interface, meaning that it waits for a clock signal before responding to control inputs and is therefore synchronized with the computer's system bus enabling higher speed. The SDRAM controller is capable of either 16-bit or 32-bit data path, and supports byte, half-word and word access. Bursts can be used for both write and read access.

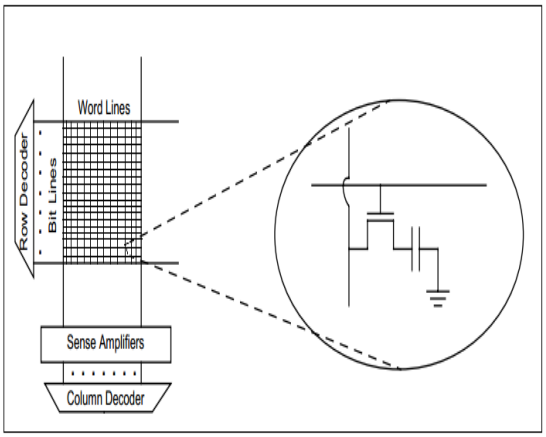

Fig.3.3. SDRAM Array structure

IV. MEMORY CONTROLLER

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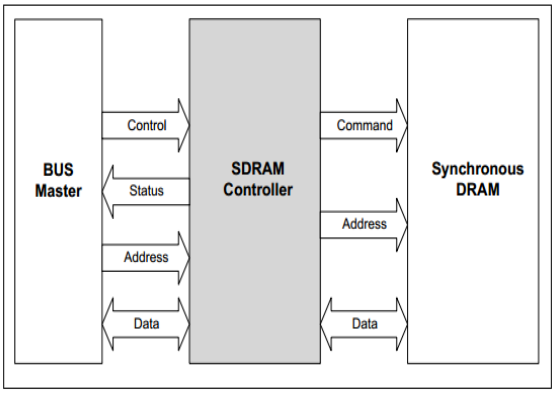

Fig.4.1. SDRAM Controller System

The controller is expected to synchronize data transfer between the processor and memory. To achieve this, the controller has to accept the requests from the processor side and convert them to a form suitable to the memory and execute the requests. Since the processor is faster than the memory, it is illogical to make the processor wait till each command is executed for it to give the next command. So the controller has to have some kind of storage so that it can buffer multiple requests while the processor continues with other work the interface at the processor side of the controller has to synchronize to the speed of the processor where as the memory side interface.

A. Operation of SDRAM controller

Only one open row in an active bank can be accessed. An ACTIVE command can open a row and make active the particular row in the memory. A PRECHARGE command issued to memory can set the SDRAM to idle state, i.e. closing the open row in this memory. If every time after accessing a row AUTOPRECHARGE command is performed, and the next access is actually involving the same row of the same bank, an ACTIVE command needs to be applied again in order to access last open row.

The memory controller basically consist of three main sub parts, they are

1) 2 Read and 2 write FIFOs
2) Command generator
3) Command scheduler

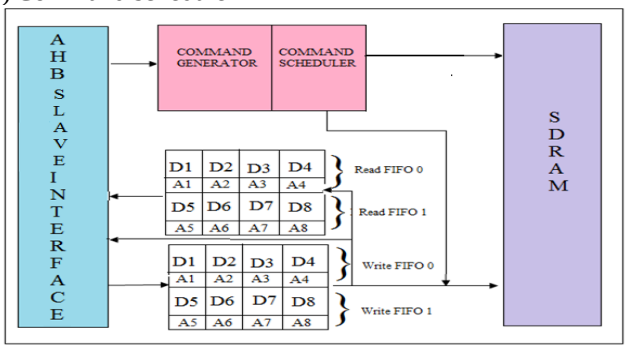

Fig.4.2. Architecture of SDRAM Controller

B. Read FIFO

After a preset number of clock cycles, the data is available on the output latches of the SDRAM for reading, and data is delivered to AHB bus and written to one of the read FIFO at the same time.

In this way, we implemented prefetching. According to the local principles of programs, the next read access is possibly a successive address to the current one. So the next data can be read from read FIFO, which can fasten the responding speed. In order to reduce the complexity of implementing read FIFO, data from SDRAM are stored in read FIFO 0 and read FIFO1 in turn.

C. Writing or ping-ponging

As it is described about the AHB, in order to reduce the responding time to write access, write FIFO are used to pack and align the data when the AHB bus data transfer size does not match the SDRAM data bus width. Based on our previous research on FPGA designs, we didn't use only one write FIFO, instead, we use 2 FIFO.

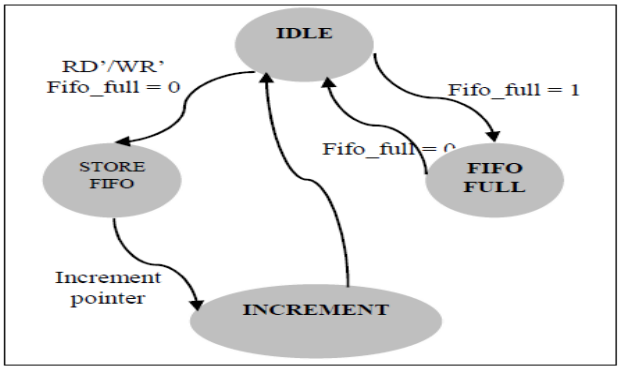

Fig.4.3. FIFO state machine

In order to keep the data consistency among the read FIFO, write FIFO and the SDRAM, whenever the data is written to write FIFO, match the write address with the addresses of data in the read FIFO. If the address matches, data will be written to read FIFO at the same time it is written to write FIFO. When reading SDRAM, match the read address with the read FIFO address and the write FIFO address first to see if the data can be read from those FIFO. This technique is called as Read-Update-Logic.

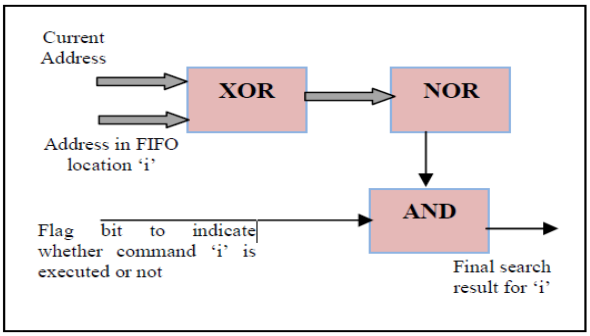

Fig.4.4. Search Logic

D. COMMAND GENERATOR

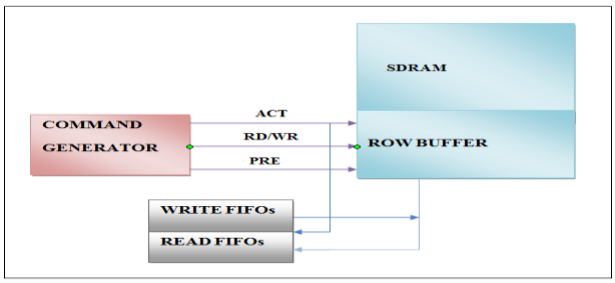

Fig.4.5. Command generator Diagram

Command generator basically generates the commands which serve

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the SDRAM without violating timing constraints. Coming to the command priorities, the read and write commands have high priority, as they put data on the bus. Recharge and activate commands have lower priorities. The command generator works on the state machine shown in the figure below to take the decision for which command has to be generated for what condition.

E. Command scheduler

The command scheduler gives the timing analysis for all the commands which are generated from the command generator. A parameter T is defined to every operation of the commands taking place as shown in the figure and the relevant timing parameters which are described for our memory.

V. ADVANCE HIGH PERFORMANCE BUS INTERFACE

AHB is a new generation of AMBA bus which is intended to address the requirements of high-performance synthesizable designs. It is a high-performance system bus that supports multiple bus masters and provides high-bandwidth operation. AMBA AHB implements the features required for high-performance, high clock frequency systems including

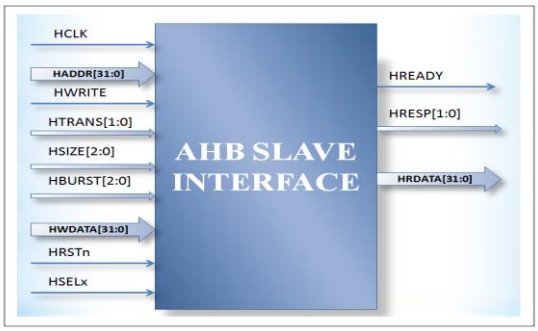

Fig.5.1. AHB slave Interface module

A. AMBA AHB signal list

This section contains an overview of the AMBA AHB signals. All signals are prefixed with the letter H, ensuring the AHB.

Table.5.1. AHB slave interface signal description

Name	Source	Description
HCLK Bus clock	Clock source	This clock times all bus transfers. All signal timings are related to the rising edge of HCLK
HRESETn Reset	Reset Source	The bus reset signal is active LOW and is used to reset the system and the bus. This is an active LOW signal.
HADDR[31:0] Addr bus	Master	The 32-bit system addresses bus.
HTRANS[1:0] Transfer type	Master	Indicates the type of the current transfer, which can be IDLE or BUSY.
HWRITE Transfer direction	Master	When HIGH this signal indicates a write transfer and when LOW a read transfer.
HSIZE[2:0] Transfer size	Master	Indicates the size of the transfer, which is typically Byte (8-bit), half word 16-bit) or word (32-bit). The protocol allows for larger transfer sizes up to a Maximum of 1024 bits.
HBURST[2:0] Burst type	Master	Four, eight and sixteen beat bursts are supported.
HWDATA[31:0] Write data bus	Master	The write data bus is used to transfer data from the master to the bus slaves during write operations. A minimum data bus width of 32 bits is recommended. However, this may easily be extended to allow for higher bandwidth operation.
HSELx Slave select	Decoder	Each AHB slave has its own slave select signal and this signal indicates that the current transfer is intended for the selected slave.
HRDATA[31:0] Read data bus	Slave	The read data bus is used to transfer data from bus slaves to the bus master during read operations. A minimum data bus width of 32 bits is recommended. However, this may easily be extended to allow for higher bandwidth operation.
HREADY Transfer done	Slave	When HIGH the HREADY signal indicates that a transfer has finished on the bus. This signal may be driven LOW to extend a transfer. Note: Slaves on the bus require HREADY as both an input and an output signal
HRESP[1:0] Transfer response	Slave	The transfer response provides additional information on the status of a transfer. Four different responses are provided, OKAY, ERROR.

B. Basic transfer

An AHB transfer consists of two distinct sections:

- The address phase, which lasts only a single cycle.
- The data phase, which may require several cycles. This is achieved using the READY signal. In a simple transfer with no wait states
- The master drives the address and control signals onto the bus after the rising edge of HCLK.

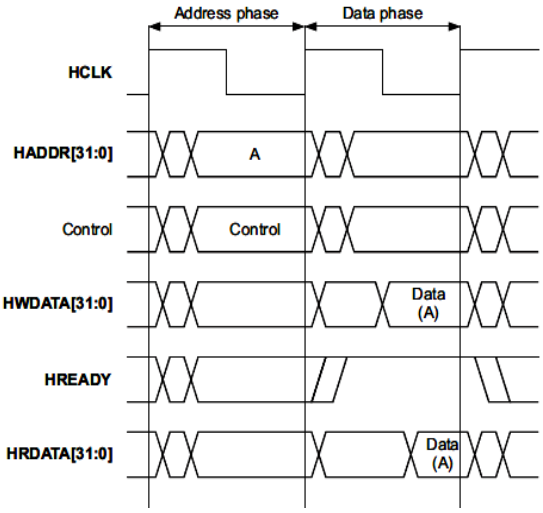

Fig.5.2. Simple transfer

VI. RESULTS

A. SIMULATION RESULTS

1. SDRAM

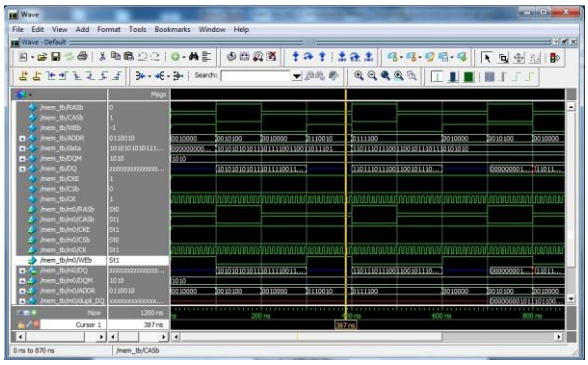

Fig.6.1. SDRAM Memory

2. Modified SDRAM Controller with FIFOing

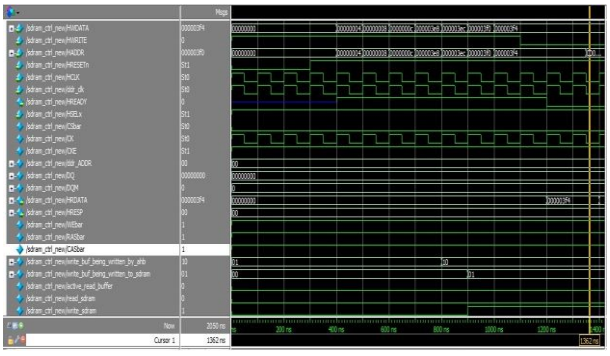

Fig.6.2. Modified SDRAM Controller

B. SYNTHESIS REPORT

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Final Results

- RTL Top Level Output File Name : amba_sdram_dump.ngr
- Top Level Output File Name : amba_sdram_dump
- Output Format : NGC
- Optimization Goal : Speed
- Keep Hierarchy : NO

9.3.4.2 Timing Summary

- Minimum period: 8.743ns (Maximum Frequency: 114.383MHz)
- Minimum input arrival time before clock : 6.914ns
- Maximum output required time after clock : 10.075ns
- Maximum combinational path delay : No path found

9.2.4.3 Timing Detail

All values displayed in nanoseconds (ns)

- Timing constraint : Default period analysis for Clock 'clk_count_261'
- Clock period : 8.743ns (frequency: 114.383MHz)
- Total number of paths / destination ports: 16101 / 1162
- Delay : 8.743ns (Levels of Logic = 5)
- Source : mc0/write_buf_write_pointer_1_1 (FF)
- Destination : mc0/write_addr_buf<1>_3_31 (FF)
- Source Clock : clk_count_261 rising
- Destination Clock : clk_count_261 rising

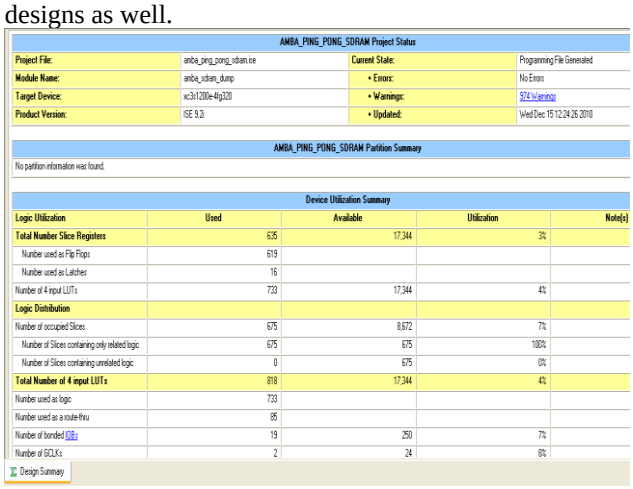
9.2.4.4 Translation Report

- Applying constraints in "amba_ping_pong_sdram_dump.ucf" to the design...
- Checking timing specifications
- Checking Partitions
- Checking expanded design
- No Partitions were found in this design.
- NGDBUILD Design Results Summary

Number of errors : 0
Number of warnings : 0

- Total memory usage is 71644 kilobytes.

Testing results between our controller and the traditional controller, the speedup rate difference is 2.1ns. Moreover, for the two SDRAM controllers, we compared the times of issuing READ and WRITE commands to off chip SDRAM while running the application program. It is shown in Table 17, running the same application program, modified SDRAM controller can reduce the times of accessing off chip SDRAM, which has a heuristic meaning for low power designs as well.



AMBA_PING_PONG_SDRAM Project Status

Project File:	amba_ping_pong_sdram.ise	Current State:	Programming File Generated
Module Name:	amba_sdram_dump	• Errors:	No Errors
Target Device:	xc3s1200e-4fg320	• Warnings:	974 Warnings
Product Version:	ISE 9.3i	• Updated:	Wed Dec 15 12:24:26 2010

AMBA_PING_PONG_SDRAM Partition Summary

No partition information was found.

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Total Number Slice Registers	635	17,344	3%	
Number used as Flip Flops	619			
Number used as Latches	16			
Number of 4 input LUTs	733	17,344	4%	
Logic Distribution				
Number of occupied Slices	675	8,672	7%	
Number of Slices containing only related logic	675	675	100%	
Number of Slices containing unrelated logic	0	675	0%	
Total Number of 4 input LUTs	818	17,344	4%	
Number used as logic	733			
Number used as a route-thru	85			
Number of bonded IOBs	19	250	7%	
Number of GCLKs	2	24	8%	

Design Summary

Fig.6.3. Synthesis Result SDRAM

VII. FUTURE SCOPE

The XDR DRAM (extreme Data Rate DRAM) memory controller can be implemented. This technology can achieve very high clock speeds. The much high speed memories can further be designed using the DDR SDRAM (double data rate SDRAM) and XDR DRAM.

VIII. CONCLUSION

An AHB interfaced high-performance SDRAM Controller has been proposed, verified and evaluated we find this SDRAM controller has high performance by taking good use of the features of SDRAM architecture and utilizing the well-known techniques such as data FIFOing and ping-ponging and burst-mode-data transfer. The testing results shows 91.66% of reduced delay with FIFOing when compared to the latency produced with FIFOing t, which is nothing but the in-built memory used within the SDRAM controller to improve its performance.

REFERENCES

1. Ching - SDRAM Controller Applications".IEEE J. Solid-State Circuits, Vol.39, Nov. 2004.Che Chung, Pao-Lung Chen, and Chen-Yi Lee "Delay-Locked Loop for DDR
2. Micron Technology Inc.Synchronous DRAM Data Sheet,2001.
3. ARM, AMBA Specification Rev.2.0, 1999.
4. "Memory Controllers for Real-Time Embedded systems" Benny Akesson Kees Goossens vol. 3, no. 3, pp. 75–77, Mar1999.
5. Hynix Semiconductor Inc., SDRAM Device operationRev.1.1, Sep. 2003.
6. Samir Palnitkar, Pearson 2nd edition "Verilog HDL, A Guide to Digital Design and Synthesis.

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