Comparative Study: MOSFET and CNTFET and the Effect of Length Modulation

Kuldeep Niranjan, Sanjay Srivastava, Jaikaran Singh, Mukesh Tiwari

Abstract*- Carbon nanotubes (CNTs) provide a number of unique feature and special properties that offers a great promise for nanoelectronic applications. In particular, the high electrical conductivity of quantum wires provides a potential solution for on-chip interconnect metals and transistors of future integrated circuits (IC's). Carbon nanotubes (CNTs) are envisioned to be used as the basic building blocks in future electronics application due to their excellent electronic properties such as high mobility, compatibility with high dielectric constants (K) and small diameters resulting in advantageous electrostatics. The purpose of this study was to develop a complete current transport model for carbon nanotube field effect transistors (CNT-FETs) applicable in the analysis and design of integrated circuits. The model was derived by investigating the electronic structure of carbon nanotubes and using basic laws of electrostatics describing a field effect transistor. Traditional MOSFET have the limitation after 60nm, So In this paper we theoretically change the channel material of traditional MOSFET with carbon nano tube (CNT) and compare the characteristics parameter. Here we found a great result like as mobility, device size Switching speed, current capacity. We compare the performance of CNTFET and MOSFET with respect to different type of gate material, effective length, and gate to source voltage. The I-V characteristic of the CNTFET is similar to MOSFET.

***Index Term:* Anisotropy, CNT-FET, Lateral Growth Work Function**

I. INTRODUCTION

In this paper work, we focus the idea about for the compare the parameter of traditional MOSFET and CNTFET. Various electrical properties like gate voltage, drain current, mobility, and device performance have been investigated. By Moore's law The dimensions of individual devices in an integrated circuit have been decreased by a factor of approximately two every two years, Traditional Silicon based MOSFET (Metal Oxide Transistor Field effect transistor) gives the better performance if sizes less than 60nm are common in the world wide research. Scaling down has faced serious limits related to fabrication technology and device performances as the critical dimension shrunk down to sub-22 nm range [1]. The limits involve electron tunneling through short channels and thin insulator films, the associated leakage currents, passive power dissipation, short channel effects, and variations in device structure and doping.

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These limits can be overcome to some extent and facilitate further scaling down of device dimensions by modifying the channel material in the traditional bulk.

For developing the better performance of the nanoelectronic device, either the shrinkage of the dimension of the existing the electronic properties of extrinsic CNT depending on their (n, m) values can be either electrically metallic or semiconductor. The band structure of carbon nanotubes results in interesting effective masses for the electrons in the tube. The velocity of the carriers in the band is related to the first derivative of the band. The electron and hole effective mass is an extensively used parameter for modeling electrical transport in semiconductor devices. The curvature of the band is thus the derivative of a constant slope, which is zero. The electrons and holes in the valence and conduction bands of a metallic nano-tube thus have an effective mass of zero.

II. THEORY AND MODELING

In silicon MOSFET, the gate contact is separated from the channel by an insulating silicon dioxide (SiO2) layer. The electrons enter and exit the channel at N source and drain contacts in the case of an n-channel MOSFET, and at P contacts in the case of a P-channel MOSFET. MOSFETs are used both as discrete devices and as active elements in digital and analog monolithic integrated circuits (ICs). In recent years, the device feature size of such circuits has been scaled down into the deep sub micrometer range. CMOS technology combines both n-channel and p-channel MOSFETs to provide very low power consumption along with high speed. New silicon-on-insulator (SOI) technology may help achieve three-dimensional integration,

The device I-V model, described below, is an attempt to include the influences of additional effects such as drain-induced barrier lowering (DIBL), source-drain parasitic resistance, and narrow channel width effects in a very compact way. The device drain current is expressed as: For $V_{ds} \leq V_{d'o}$ (triode region), the I-V characteristic of the N- and P- type transistor in the non-saturated and saturated region are represented in fig.1 (with the SPICE circuit for obtaining these characteristic for an n transistor).That we use the absolute value of the voltages concerned to plot the characteristic of the P-and N-transistor on the same axis. The boundary between the linear and saturation regions corresponds to the condition $|V_{ds}| = |V_{gs}-V_t|$, and appears as a dashed line in Fig.1.The drain voltage at which the device become saturated is called $V_{dsat,}$ or the drain, saturation voltage. In the above equation that is equal to $V_{gs}-V_t$ .Ids varies linearly With Vgs and V_{ds} when the quadratic term $V^2_{ds}/2$ is very small [2].

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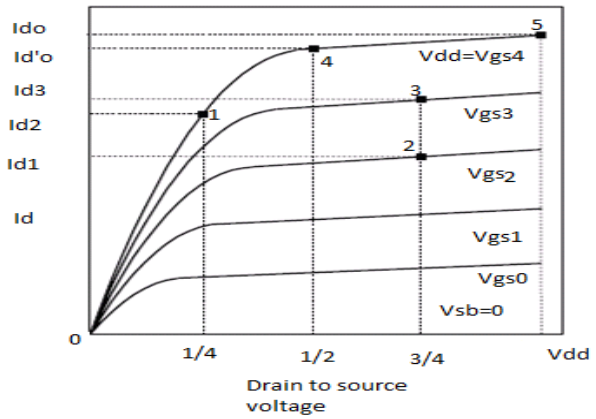

Fig.1: I-V characteristic [2]

III. RESULT & DISCUSSION

MOSFET Parameter: The drain current of MOS transistor can be described by the following equation (1) [3]
Here we use 4th order low pass filter is designed to demonstrate the performance of this differentiator. In the saturation region-channel is strongly inverted and drain current flow is ideally independent of drain source voltage (source inversion region) [4].

$$I_d = \beta(V_{gs} - V_t)^2 / 2 \qquad 1$$

And C_{OX} is oxide capacitance V_{gs} is the gate to source voltage, V_t is the device threshold voltage, and β is the MOS transistor gain factor, the last factor is dependent on both the process parameter and the device geometry and is given by

$$\beta = \frac{\mu\varepsilon(w/l)}{t_{ox}} \qquad 2$$

Here μ is the effective surface mobility of the carrier in the channel, ε is the permittivity of the gate insulator, t_{ox} is the thickness of the gate insulator, w is the width of the channel and, 'l' is the length of the channel [5] . The gain factor β thus consist of the process dependent factor $\mu\varepsilon / t_{ox}$ .When an MOS device is in saturation, the effective channel length actually is decreased such that

$$L_{eff}=L-L_{short} \qquad 3$$

Where

$$L_{short} = \sqrt{2\frac{\varepsilon_{si}}{qN_A}(V_{dS} - (V_{gS} - V_t))} \qquad 4$$

Where q is the charge of electron and N_A is the doping concentration density of the substrate. The modulation of length depends upon (1) material property i.e., dielectric constant, capacitance and the number of dopant (II) processing characteristics. The reduction in channel of length 'l' increases the (W/L) ratio thereby increasing β as the drain voltage increases, thus rather than appearing as a constant current source with infinite output impedance, the MOS device has finite output impedance an approximation that take behavior into account is represented by the following equation [6,7],

$$I_d = \frac{k}{2}\frac{W}{L}(V_{gs} - V_t)(1 + \lambda V_{ds}) \qquad 5$$

Where k is the progress gain factor $\mu\varepsilon / t_{ox}$ and λ is empirical channel length modulation factor having a value in range 0.02 to 0.005 V^{-1}. and Φ_p is strong inversion surface potential. The γ is the constant that describes the substrate bias effect. The typical values for γ lie in the range of 0.4 to 1.2. It may be expressed as

$$\gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{Si}N_A} = \frac{1}{C_{ox}}\sqrt{2q\varepsilon_{Si}N_A} \qquad 6$$

The mobility, μ, describes the ease with which carries drift in the substrate material. It is defined by $\mu = \frac{v}{E}$ where v is the drift velocity and E is the applied electric field.

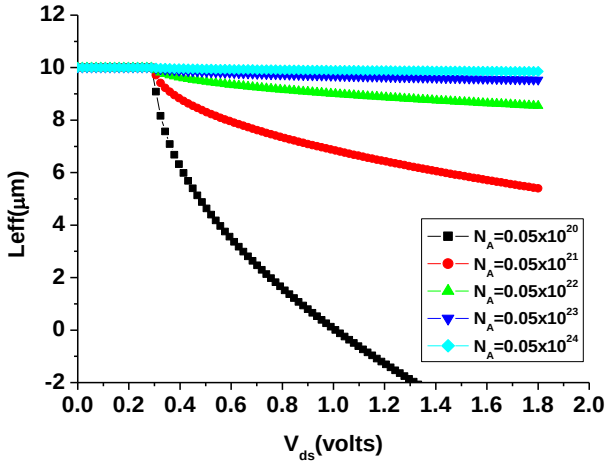

Fig.2: Variation of L_{eff} with doping concentration

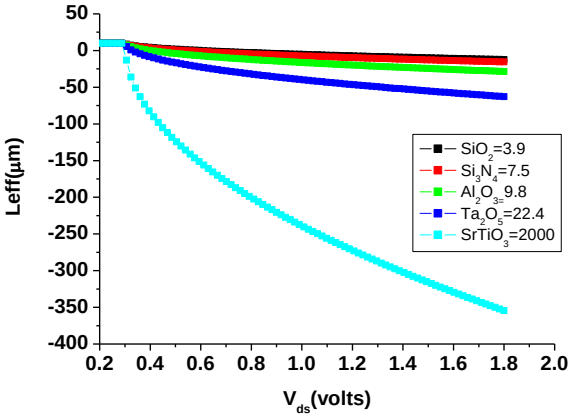

Fig.3: Variation of L_{eff} with different type of the dielectric material

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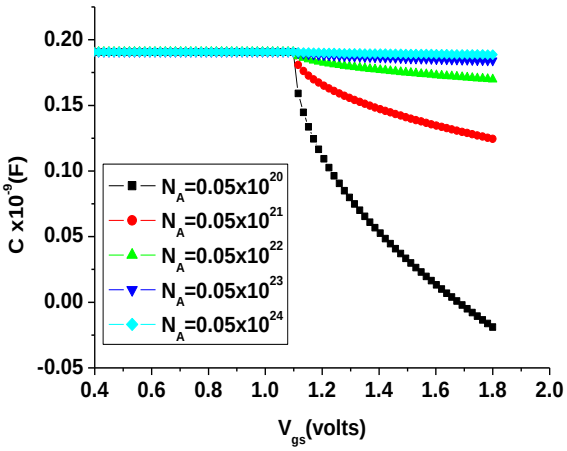

Fig.4: Variation of Cox with different doping

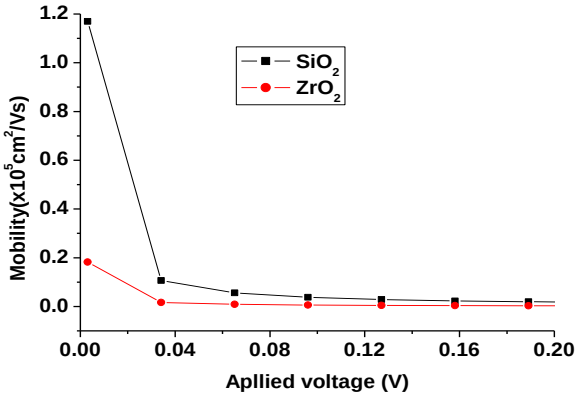

Fig.5: Variation in mobility with different dielectric material

CNTFET Parameter

A carbon nanotubes bandgap is directly affected by its chirality and diameter. If those properties can be controlled, CNTs would be a promising candidate for future nano-scale .The length of C_h is thus the circumference of the tube, and the radius is given by the formula

$$R_t = \frac{|C_h|}{2\pi} = \frac{acc}{2\pi}\sqrt{3\left(n^2 + m^2 + nm\right)} \quad 7$$

Where, for example, $R_t \approx 0{:}63$nm for a (16, 0) nanotube Fig5 , Depending on their (n, m) indices, nanotubes are placed in one of three groups, which are named according to the shape of the cross-section established by the chiral vector slicing across the hexagonal pattern: armchair (n= m and $\zeta = 30^o$), Zig-Zag (m = 0 and $\zeta = 0^o$), and chiral (all other cases), where ζ is the angle between C_h and $\hat{a}_1$. The indices also serve to quickly identify the conduction properties of a nanotube-when (n- m) is a multiple of 3, the nanotube is metallic, and otherwise it is semiconducting. The structure of a carbon nanotube (CNT) is that of a graphite layer rolled into a closed cylinder. The number of atoms per nanometer-length on a single-wall nanotube can be estimated by the formula

$$N_{atoms} \approx 2\frac{A_{cyl}}{A_{hex}}\frac{1}{L_t} = \frac{8\pi R_t L_t}{3\sqrt{3}a_{cc}2}\frac{1}{L_t} \approx 240R_t \quad 8$$

Where A denotes area, and R_t and L_t are, respectively, the tube radius and length in nanometers. Since a typical tube used in the devices examined in this thesis will have dimensions of $R_t \approx 0{:}63$ nm, we expect to have an atom density of roughly 150nm^{-1} contributing to the conducting "cloud" [8].

The dispersion relation for graphene, obtained by the Slater-Koster tight-binding scheme, considering only π-orbital's, and following the lattice vector conventions is given [9, 10, 11].

$$E_{graphene}(k_x,k_y) = \pm t\left[1 + 4\cos\left(\frac{\sqrt{3}k_x a_{cc}}{2}\right)\cos\left(\frac{\sqrt{3}k_y a_{cc}}{2}\right) + 4\cos^2\left(\frac{\sqrt{3}k_y a_{cc}}{2}\right)\right] \quad 9$$

The nanotube dispersion relation is then given by

$$E_{graphene}(k_x,k_y) = \pm t\left[1 + 4\cos\gamma_1\cos\gamma_2 + 4\cos^2\gamma_2\right] \quad 10$$

Graphene is thus a zero-band gap conductor, but going from two dimensional flat graphene to a rolled carbon nanotube can change that.

However, as will be shown later, a smaller band gap allows for greater carrier densities on the tube under certain conditions, and thus higher currents.

$$E_g = \frac{|t|a_{cc}}{2R_t} \quad 11$$

The band gap is thus a geometrically-tunable property, and given that we can make devices by choosing nano-tubes by their approximate radius (presently via scanning tunneling microscopy), we may be able to exploit this tenability in nano-electronics. We can determine the size of the gap for a semiconducting tube where (n-m) is not divisible by 3. Chiral number is the important parameter to affect the capacitance of the oxide layer. In fig.6, and Fig.7 At 50 nm oxide thickness for long channel length CNTFET show the variation of the oxide capacitance with chiral number. The lower chiral number shows the higher capacitance between the oxide layer and the CNT channel. The alternation of the channel length is supposed to be brought by the removal of dielectric layer.

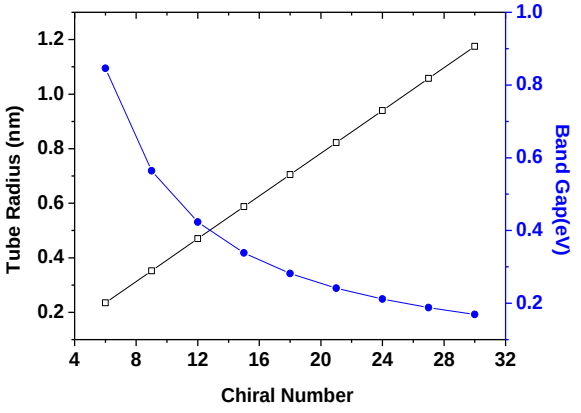

Fig.5: Variation of Tube radius and Eg with chiral Number (Zig-Zag (m = 0 and $\zeta = 0^o$))

This is due to channel length in between the source and drain. Due to removal of the layer, the CNT are stretched along the concave shape. The main part of the CNT remains contact with the substrate surface

instead of hanging across the electrode gap, because there is no filed effect in the transistor with suspending channel. The etchings of the oxide layer from the substrate in the dramatic Long channel the higher values of the capacitance as Discuss [12].

Thin films of high-κ materials, such as ZrO2 and HfO2 (κ ~ 15–25), are highly desirable for gate dielectric integration in field effect transistors as they enable high ON-state current densities (speed) and low operating power consumptions. The lack of dangling bonds at the nanotube/high-κ interface and the weak noncovalent bonding interactions between the two materials, prevent any large perturbation of electron transport in carbon nanotubes. The integration of high-κ dielectrics, however, has been a challenging problem towards many researchers in planar MOSFETs because of the inherent mobility degradation of the Si channels.

In CMOS FETs, the gate capacitance is actually the series combination of three terms, the oxide capacitance, the depletion capacitance of the gate electrode, and the capacitance to the carriers in the Si channel [13], In CNTFET there are capacitances add a

$$1/C=1/Cox+1/C_{gate}+1/C_{Si}. \quad 12$$

As C varies as $1/t$, capacitances in series can be represented by a sum of effective distances. Thus we can define an 'effective capacitance thicknesses (of SiO_2) as

$$ECT=EOT+t_{gate}+t_{Si}. \quad 13$$

The channel capacitance arises because quantum delocalization of the two-dimensional electron gas of electrons means that these electrons cannot lie infinitely close to the channel surface, but must delocalize a few Angstroms into the channel. On the other hand, the gate electrode is presently made out of degenerately doped polycrystalline silicon, for engineering convenience. Thus, its low carrier density gives a depletion depth which is a few ˚A, whereas a good metal has a higher carrier density and has a depletion depth of only 0.5 ˚A. This depletion effect can be removed by replacing the poly-Si with a normal metal. Typical metals for this use could be TiN, TaSiN and Ru. The metal is chosen primarily for its work function. One of the utmost significant developments in devices fabrication is that the gate dielectric has moved from silicon dioxide (SiO_2) to high-κ dielectrics such as ZrO_2, HfO_2, and Al_2O_3, which delivers high-performance transistors with low voltage and possibly hysteresis-free operation.

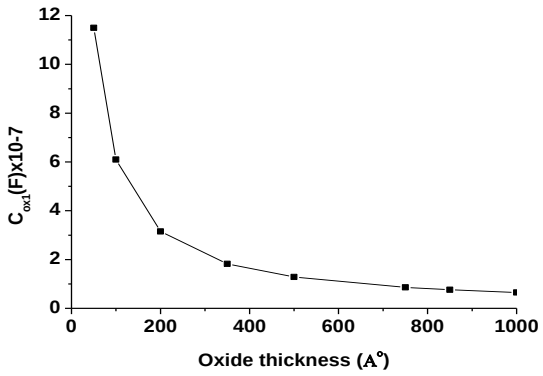

Fig.6: Variation of the oxide capacitance with the oxide thickness.

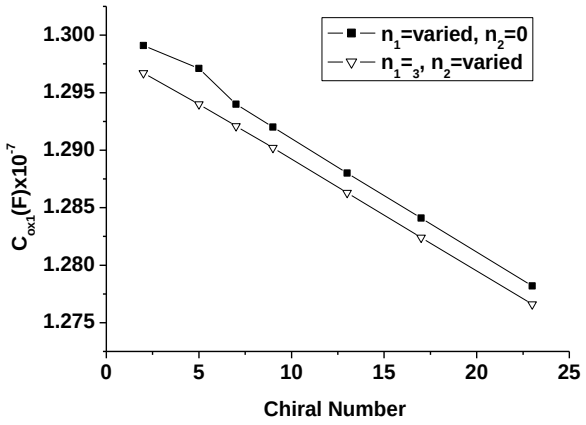

Fig.7. variation of the oxide capacitance with the chiral Number of the CNT

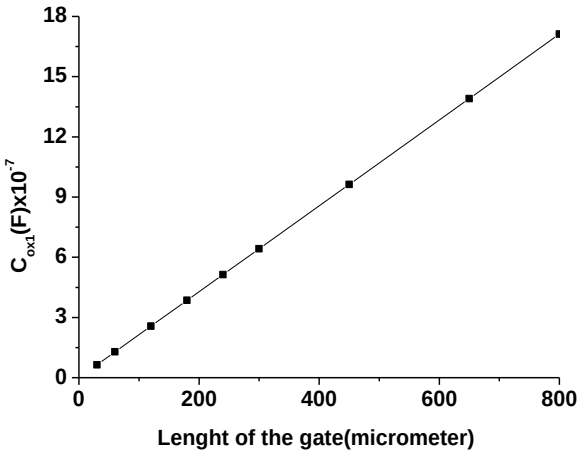

Fig.8: Variation of the oxide capacitance with the length of the gate (for (10, 10)

At 100mV, Fig.9 shows the behavior of mobility of electron between the CNT channel (5μm, of (10, 10)) and dielectric interface of the different materials. The mobility of the electron get reduces with increase the dielectric constant of the materials. SiO2 provides the better path for the electronic transport between the electronic channel and dielectric layer as compared to other high-κ dielectrics. This effect can be seen in channel length modification of the CNT with chemical etching, which enhance the mobility of the electron between channels. Higher mobility is obtained at long channel length of the CNT between the source and drain which shows the linear relationship as shown in Fig.9.

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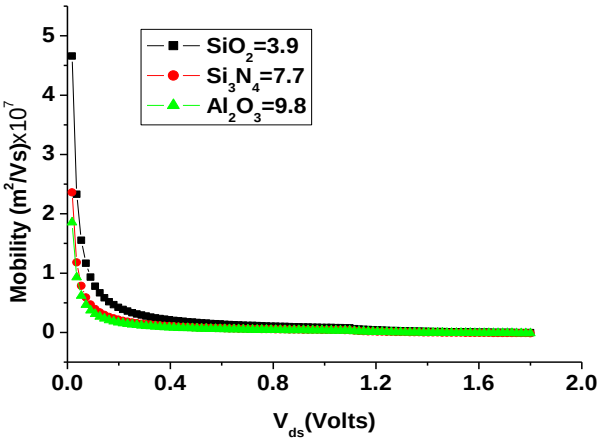

Fig.9: Variation of the mobility with channel length (micrometer) of the CNT.

IV. CONCLUSION

The channel of traditional MOSFET will replace by CNT .In MOSFET when we shrunk the side 20nm then face the serious limit like short channel, power dissipations and electron tunneling, face the problem from MOSFET channel. The CNT was used as channel in between the source and drain because of high mobility. A better I-V characteristic was obtained with higher mobility in between the channel and used dielectric layer. Length of the channel modifies the mobility as well as the oxide capacitance of the CNT channel. Substrate etching can make the device thinner and lighter without losing the performance. Higher channel length provides the better mobility at the thinner cantilever of the SiO2 dielectric layer. CNTFET is the best device for future very large scale intrigation (VLSI). In this paper result shows CNTFET gives the high mobility 300 times faster than MOSFET.

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