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A New Technique of Developing a CPLD Based System for Wireless Device Control through Mobile Phone

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Abstract— Sometimes it is very much essential to control the home appliances and different devices from a far distance. This paper gives an idea of developing a system which will enable user to control from a remote using a mobile phone based interface. Within the large coverage area of the service provider mobile phone is used to control the devices which may be located geographically far apart. CPLD is used here to direct the interfacing circuitry either to switch on or off the devices connected with it. CPLD based system is used due to faster implementation and hardware verification facilities. The device is programmable and reconfigurable. This is one of the most powerful advantages of using the device where the program is to be changed frequently for some specific applications. The functions associated with the assigned keys are stored in the CPLD. It processes the data coming from the output of a DTMF decoder and generates the output according to the key pressed from the mobile phone at the transmitting end. Xilinx 9.2i software is used to write the program in VHDL and the hardware is implemented with the help of VLSI trainer kit (Model: UNI-BSX-M1, Manufacturer: Milman).

Index Terms—CPLD, DTMF decoder, Mobile phone, TRIAC, VHDL, Zero crossing detector.

I. INTRODUCTION

With the advent of modern technology home and office appliances like Lights, Fan, refrigerator, Air cooler, Computer, TV, washing machine, motor drives, furnace temperature monitoring system etc. demands switching remotely [2]. Among various techniques used to control the devices or home appliances, CPLD based system is one of the best constructs because the program can be modified and simulated again and again until the best simulated result is obtained. Device switching through CPLD and the mobile phone have a number of advantages over the system designed with microprocessor or microcontroller [1] [3]. They can handle large design complexity. VHDL can be considered as an integrated amalgamation of the five languages. These are sequential language, concurrent language, net-list language, timing specifications, waveform generation language. It specifies concurrent as well as sequential behavior to describe the digital system with or without timing [5]. With the advent of computer based design methods and tools, the design process transfer to the computer using Electronic Design and Automation (EDA) tools. The program is written in Hardware description language with the help of software development tool.

Generated test waveform provides the timing correctness of the design. With the help of it detailed structure of the design will be automatically generated. Thus VHDL reduces implementation time cost and manpower [4]. Therefore our design comprises CPLD based system. For implementing a circuit which supports so many inputs and outputs a sophisticated type of chip, called a Complex Programmable Logic Device (CPLD) provides the alternate method of using multiple PLAs or PALs. Fig. 1 shows four PAL like blocks that are connected to a set of interconnection wires. Each PAL like block is also connected to a sub circuit labeled I/O block, which is attached to a number of the chip's input and output pins[4] [10].

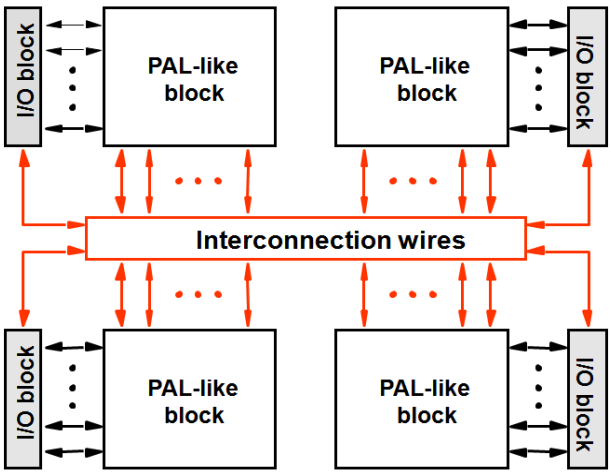

Fig. 1: Architecture of the CPLD

The device is build around one popular Dual Tone Multi frequency (DTMF) decoder which produces the output in 4-bit binary number for a particular button pressed by the user at the transmitting end. It feds the output to the CPLD which takes the decision whether to switch on/off the devices connected with the interfacing Circuits.

II. PRINCIPLE OF SYSTEM DEVELOPMENT

The system may be viewed as the integrated merger of hardware and the software. Hardware is divided into three different functional units. First unit receives the instruction and decodes it. Second unit is designed to process and execute the instruction. Third unit is responsible for switching the home appliances or office automation equipments [2].

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Here the system is developed for switching of seven different devices. The number is not restricted to seven. The Program may be changed and hardware can be modified to include more devices later. They may be switched ON or OFF individually or simultaneously after pressing particular mobile buttons assigned for the specific applications. When a call is initiated from the user mobile phone the mobile connected at the receiver end responds immediately because it is in auto answer mode [2]. The DTMF decoder decodes the code which is recognized by the CPLD [10]. It generates the output either high or low accordingly. The device switching is thus achieved by the Triacs and their Driver circuitry. Fig. 2 shows the block diagram of the composite unit.

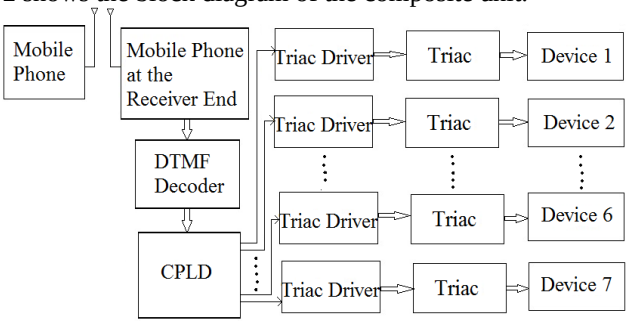

Fig. 2: Block Diagram of the proposed CPLD based system

III. FUNCTIONAL DESCRIPTION

In this method of designing a CPLD based system the mobile takes an important role. This is connected at the receiver end with its auto answer mode setting. When a call is established any button pressed at the user end generates dual tone multiple frequency (DTMF) at the other end. DTMF consists of two pure tone (pure sine wave) sound and the frequency is allocated by CCITT [1] [6]. The received tone is processed to generate with the help of a popular DTMF decoder KT3170. The DTMF decoder produces two different frequencies. One is from lower band and other is from upper band frequencies. For an example pressing of a key '9' produces a tone consists of 852 Hz from the low group and 1477 Hz from the high group of frequencies. The architecture specifies that there is a band split filter section which separates the high and low group tones. The digital counting section after the band split filter section generates a particular four bit binary number. The counting section verifies the received tones before passing it to the related bus [8]. This binary equivalent number makes the selection of the devices to be switched ON/OFF. The VHDL program runs immediately after receiving the sequence. We have used CPLD of Family: XC9500, Device: XC9572, Package: PC84.

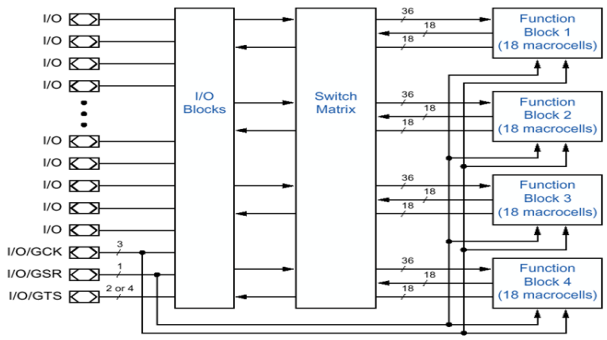

Fig. 3: Architecture of CPLD of Xilinx 9500 - family

CPLD is programmed to take decision of changing the state of the connected devices. The layout of the keypad used in a mobile handset is shown in the table I [1].

Table I: DTMF keypad and associated frequencies

Frequency	1209 Hz	1336 Hz	1477 Hz	1633 Hz
697 Hz	1	2	3	A
770 Hz	4	5	6	B
852 Hz	7	8	9	C
941 Hz	*	0	#	D

Table II: Function Table of DTMF decoder KT3170

Low Group Freq. (Hz)	High Group Freq. (Hz)	Digit	Binary Output			
			Q4 (MSB)	Q3	Q2	Q1 (LSB)
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0
--	--	ANY	Z	Z	Z	Z

All of the keys shown are used here to change the status of the devices. The DTMF decoder produces 16 different values of the binary output Q4Q3Q2Q1 [8]. Upper group and the lower group frequencies corresponding to the DTMF keys are shown in Table II. For switching ON the devices a set of the keys are used which are normally the odd number and alternate letter keys for the sake of simplicity.

Table III: Functions of mobile keys for switching ON

Key pressed by user	Action performed
1	Switch ON: Device1
3	Switch ON: Device2
5	Switch ON: Device3
7	Switch ON: Device4

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9	Switch ON: Device5
A	Switch ON: Device6
C	Switch ON: Device7
*	Switch ON: All Devices

The keys assigned to switch OFF the devices are normally even number and the next letter to the assigned letter keys selected for switching ON the devices. So the Key (1-2), (3-4), (5-6), (7-8), (9-0), (A-B), (C-D) make the pair for the respective devices. * and the # buttons are used to switch ON and OFF all the devices at the same time respectively. Function of the keys for Switching ON and OFF the devices are shown in table III and table IV.

Table IV: Functions of mobile keys for switching OFF

Key pressed by user	Action performed
2	Switch OFF: Device1
4	Switch OFF: Device2
6	Switch OFF: Device3
8	Switch OFF: Device4
0	Switch OFF: Device5
B	Switch OFF: Device6
D	Switch OFF: Device7
#	Switch OFF: All Devices

Interfacing of the electrical appliances to the CPLD is obtained through the interfacing circuits consists of zero-cross optoisolators Triac driver, MOC3041 and Triac BT136. IC MOC3041 comprises of GaAs infrared light emitting diode optically coupled to a monolithic silicon detector performing the zero crossing Triac driver. This is used with BT 136 in the interface of logic systems to equipment powered from AC lines, such as industrial control, motor, solenoids, consumer appliances, lighting control, static power switches, AC motor drives, solid state relays, EM contactors etc [9].

IV. SIMULATION & RESULT

For successful physical implementation of the system a number of different steps and verification stages are to be covered. The design flow starts with design entry through HDL code. Here the VHDL code is written with the help of Xilinx 9.2i software using the behavioral style of modeling design style. RTL level is generated using high level of synthesis process. Then the RTL level is further translated and converted to gate level net list of the design through Logic level synthesis. This is the connectivity description of the designed gate level circuit. After synthesis EDA tool generates EDIF/XNF file. The next process of the design flow is gate level simulation through which the functionality of design is verified after synthesis. Required number of input signals is applied and the output signals are checked. If anything wrong with the simulated result or the functionality of the system to be modified then the HDL code is to be changed at the entry level. The next process is placement and routing. Before doing this user constraint file (UCF) is created. This describes the input and output pin assignment of the CPLD. Finally Programming is the most important part of the design flow. Here the actual digital design is transferred to the target device [1] [3]. Fig. 4 shows the design flow of any VHDL based system.

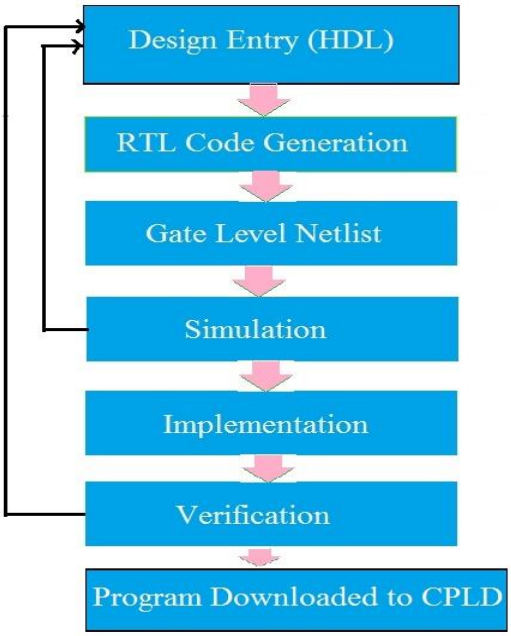

Fig. 4: Design flow using VHDL

Programming technique using flowchart is shown in fig. 5.

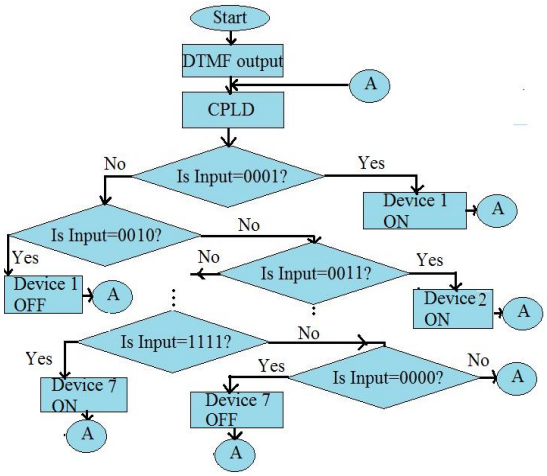

Fig. 5: Flowchart of the main program

Programming is the process of transferring the final .jed file generated by the tool to the CPLD. JTAG cable is used for interfacing the device with the PC. Due to the ISP technique used to program the CPLD, Joint Test Action Group (JTAG) port is given with the CPLD board. JTAG port is standardized by IEEE. It uses a non-volatile of programming technology. In case of power failure the CPLD can retain the program [1].

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Resource summary of the used CPLD family XC9500 is given in fig. 6.

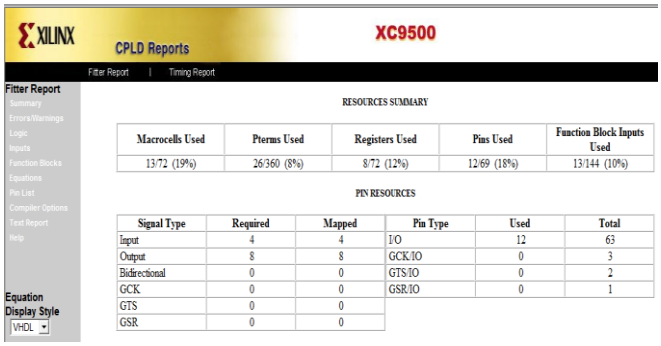

Fig. 6: Design summary using CPLD XC9572

The resulting simulation for a set of keys pressed from the user mobile is shown in fig. 7. It shows the output state of CPLD for the input applied through the DTMF decoder.

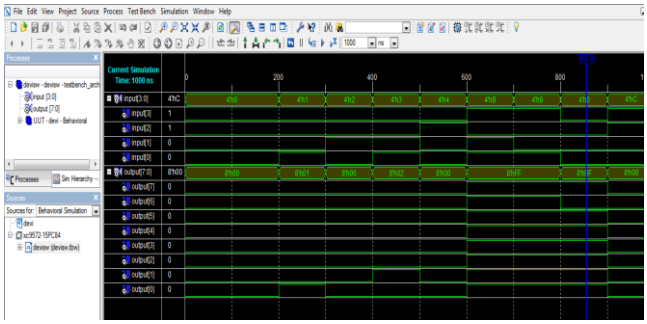

Fig. 7: Simulation result for pressing of a particular set of keys from the user mobile

V. CONCLUSION

This paper gives the idea of reception of the mobile code and application for specific purposes. Sometimes we forget to switch of home appliances while leaving for a journey. This leads to the wastage of power, money and often damage of the device due to overheating. Even if we remember, it may not be possible to come back and switch off the devices again. The idea of developing the system gives a solution because it uses the mobile phone without which we can't move a little bit. It also gives a solution to the bed ridden patient, children who can't reach to the switch board.

VI. ACKNOWLEDGMENT

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