Reliability Prediction for Low Power Adiabatic Logic Families

Suresh Kumar Pittala, Swajeeth Pilot. Panchangam, A. Jhansi Rani

Abstract*— This paper focuses on predicting reliability of low power adiabatic logic families. Reliability logic diagram for each logic family is briefly discussed. Power dissipation is an important aspect of digital computing systems because of the increasing demand for portable electrical digital systems. Unlike conventional CMOS logic circuits, adiabatic circuits recover and reuse circuit energy that would otherwise be dissipated as heat and thus improve the portability of system. Development of adiabatic logic as an approach to reduce the energy dissipation of the digital circuits has became a major focus of interest over the last one decade. In this paper, we performed simulations at the schematic level using a standard 0.18 µm CMOS technology. The performance and power dissipation of the logic styles are evaluated for a maximum frequency of operation of 100MHz.

Index Terms*— Reliability prediction, Adiabatic system, low power digital system, CMOS logic circuits, Power dissipation.

NOTATIONS

FPMH Failures per million hours
λ Failure rate
PC Power clock
MN NMOS
MP PMOS
λ_{net} Net failure rate

I. INTRODUCTION

Low power dissipation is a primary design criterion of digital systems because of the increasing demand for computing systems like lap top computers, cellular phones, personal digital assistant (PDA) and any kind of portable electronic device [3], [4]. Such systems require highly reliable components to avoid unexpected failures which might result in huge economic loses apart from ill effects on environment, health & safety of human beings and other species. Instead of spending huge amounts on replacement/repair of industrial systems due to unreliable components it may be better to have a high reliable system with adequate redundancies. An attempt is made in this paper to predict the reliability of each logic family. To date, all microchips have been designed to dissipate the entire amount of electrical energy drawn as heat. The central idea of heat removal for high-performance systems is to recover system energy that would otherwise be dissipated as heat. Any reduction in energy consumption, even at the cost of increased circuit complexity, must be pursued to improve the system performances in terms of portability. Furthermore, the number of gates per chip has been doubled for every eighteen months according to Moore's law [5], but the gate switching energy has not been reduced at the same rate. As a result, the power consumption of high-performance chips has increased and it has become harder to remove the produced heat even with sophisticated and expensive cooling systems.

The rest of the paper is organized as follows:

In Section-2, the problem statement and brief introduction to adiabatic switching analysis are presented. In Section-3, the reliability logic diagram to each logic family is presented. In Section-4, the reliability prediction method for constant failure rate components is briefly discussed and the results are tabulated. Conclusions are presented in section-5, followed by selected references.

II. LOW POWER ADIABATIC SYSTEM

2.1. Problem statement

Power dissipation is an important aspect of digital computing systems because of the increasing demand for portable electrical digital systems. Unlike conventional CMOS logic circuits, a new design needed to be adopted to recover and reuse circuit energy that would otherwise be dissipated as heat and thus improve the portability of system. These designs have to be effectively designed, developed, and implemented to achieve high reliability for the use in computing systems like lap top computers, cellular phones, PDA and any kind of portable electronic device.

In this paper, we focused on two important aspects. Our first research objective is to predict the reliability of each adiabatic logic family. Second research objective is to simulate, evaluate the power dissipation in each logic family and obtain the best low power dissipating adiabatic logic family.

2.2. Standard switching in conventional CMOS

Let us examine how energy is dissipated during a switching transition in standard CMOS circuits. Fig. 1 shows a simple *RC* tree. The transition of a circuit node from LOW to HIGH can be modeled as charging the *RC* tree through a switch from a constant voltage source. When the switch is closed, there is a flow of current through the circuit and the capacitor charges exponentially to V_{dd}.

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Suresh Kumar Pittala, Associate Professor, Department of ECE, DVR & Dr. HS MIC College of Technology, Kanchikacherla, A.P, India-521180.
Swajeeth Pilot. Panchangam, M. S, Reliability Engineering Centre, Indian Institute of Technology, Kharagpur, West Bengal, India-721302.
Dr. A. Jhansi Rani, Professor, Department of ECE, V.R. Siddhartha Engineering College, Vijayawada, A.P, India-520007.

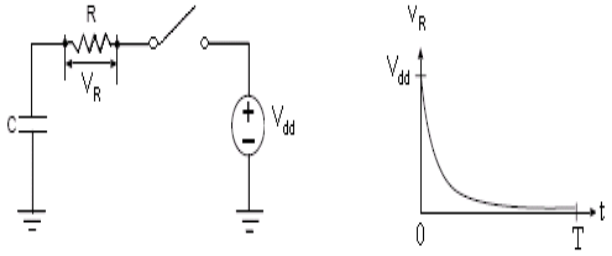

Fig.1. Charging an RC tree with a switch

The energy taken from the power supply is CV^2_{dd}. Out of this, only ½ CV^2_{dd} is stored in *C* and the other half is dissipated in *R*. The energy dissipated is independent of the value of *R*. During the discharge of the node, the energy in the capacitor is dissipated in the discharging resistor. Over a complete cycle of a charging and discharging of the node, energy of CV^2_{dd} is drawn from the source and is dissipated to the surroundings. To reduce power dissipation, one natural approach is to decrease transistor sizes or reduce the supply voltage or minimize the switching activities. Scaling analysis shows that transistor size shrinking would not achieve significant benefits in power dissipation, if one insists on conventional CMOS. Switching activities in many circumstances, cannot be reduced either. The reduction of supply voltage is thus, the best alternative for decreasing power consumption significantly. Voltage scaling also has a natural limit - supply voltage levels cannot be dropped to the point where signal levels are indistinguishable from noise.

2.3. Adiabatic switching and energy recovery

Adiabatic switching [1] can be achieved by ensuring that the potential across the switching devices is kept arbitrarily small. In fig.1 it can be seen that the potential drop (V_R) across the switch resistance is high over some time interval in the conventional case because of the abrupt application of V_{dd} *to* the *RC* circuit. Fig.2 shows the adiabatic charging in an *RC* tree.

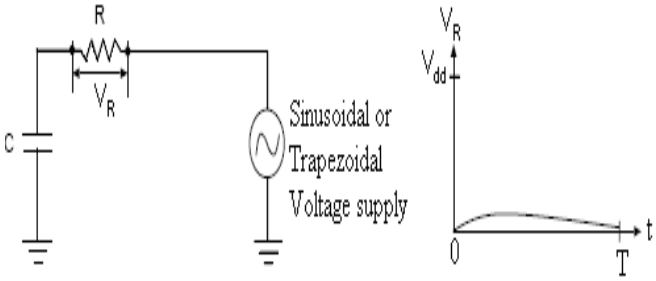

Fig.2. Adiabatic Charging an RC tree.

Adiabatic charging may be achieved by charging the capacitor from a time varying source that starts at 0 V. The voltage ramps to V_{dd} at a slow rate that ensures that voltage across the resistance *is* kept arbitrarily small at all times. This rate is set by ensuring that $T >> RC$, where T is duration of the ramp.

In fact, for $T >> RC$, the energy dissipated is given by eq. (1)

$$E_{resistance} = \frac{RC}{T} * C * V^2_{DD} \quad \text{..... (1)}$$

An increase in *T* causes a decrease in power dissipation. Now if *T* is sufficiently larger than *RC*, energy dissipation in the resistor during charging tends to zero and so the total energy taken from the supply is $CV_{dd}^2/2$, which is the minimum, required to charge the capacitor and to hold the logic state. This stored energy in the output node can be returned to the power supply during the discharge cycle if it too is performed adiabatically. As a result with a suitable supply, it should be possible then to charge and discharge signal node capacitances with only marginal net losses.

There are two fundamental rules which the adiabatic logic circuits should follow [6]:

- A transistor is never turned on when there is a significant voltage drops across its source and drain terminals.
- A transistor is never turned off when there is a significant current flowing through its channel.

Violation of any of two rules mentioned above, results in significant power dissipation. With careful design, individual transistors can operate in a nearly adiabatic fashion. However, it is not an easy task to have all the circuit elements working in adiabatic fashion. This is because a gate in a latter stage is controlled by gates in earlier stages. Thus, a gate not only should switch adiabatically, but also operate in such a way that the subsequent gate(s) can switch adiabatically. The design task for adiabatic circuits is to ensure that every element in the circuit work together in a nearly adiabatic fashion.

III. RELIABILITY LOGIC DIAGRAM AND PREDICTION FOR LOW POWER ADIABATIC LOGIC FAMILIES

Reliability Block Diagram (RBD) is alternatively called Reliability Logic Diagram (RLD). RBD/RLD are diagrams drawn with boxes (may be square or rectangle) and lines to represent the functional relationship between components of an assembly or system. Boxes represent the components and line indicates the functional connections between components.

Reliability evaluation and assurance at the design stages are essential for design improvement, and subsequent approval and therefore the only method of doing this is the RLD. Series, parallel, series-parallel, parallel-series, non-series-parallel, k-out-of-n, and networks are some generally used reliability block diagrams.

Adiabatic logic families can be broadly classified into two major groups: (1) diode based and (2) transistor based. The focus of research is more on transistor based adiabatic circuits compared to diode based ones because of their inherently less dissipative nature and ease of fabrication and integration. Transistor based adiabatic circuits are again classified into two groups:

- Fully adiabatic logic family.
- Partially adiabatic logic family or Quasi-adiabatic logic family

Some of the transistor based adiabatic logic families are discussed below.

3.1. 2N2P logic family

This belongs to the quasi-adiabatic logic family, which is also known as Efficient Charge Recovery Logic (ECRL). More popularly known as 2N2P, the name is based on the convention of using the number of transistors in a gate because

the cost for each input in terms of transistors is two NMOS transistors and the overhead for each complete gate is two PMOS transistors. The circuit uses differential logic, so each gate computes both a logic function and its complement, and each gate requires complimentary inputs. The basic circuit for an inverter-buffer is shown in Fig.3. The cross-coupled PMOS transistors are connected to the power clock supply (PC).

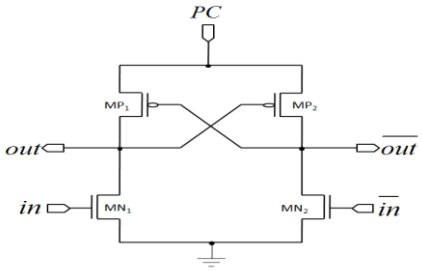

Fig.3. 2N2P inverter/buffer

Reliability logic diagram for the 2N2P family is as shown in fig.4.

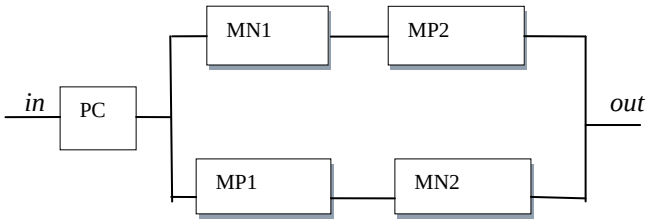

Fig.4. RLD for 2N2P family

3.2. 2N-2N2P logic family

A variant of the ECRL logic family is 2N-2N2P family, the only difference is that 2N-2N2P has a pair of cross-coupled NMOS transistors in addition to the cross-coupled PMOS transistors common to both families as shown in fig.5 2N-2N2P thus has cross-coupled full inverters and thus is very similar to a standard SRAM cell. The timing and logical operation of 2N-2N2P is identical to that of 2N2P.

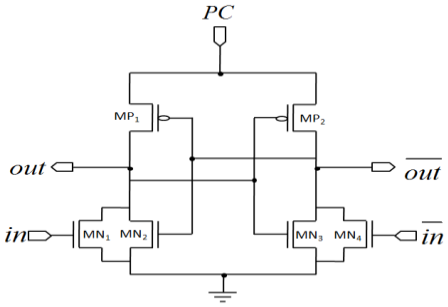

Fig.5. 2N-2N2P buffer/inverter

Reliability logic diagram for the 2N-2N2P family is as shown in fig.6.

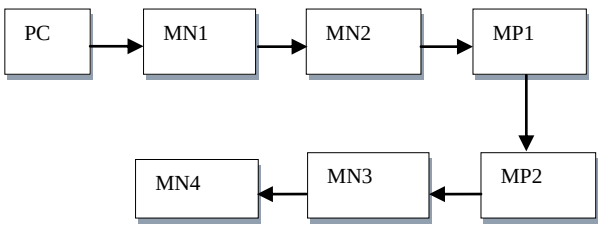

Fig.6. RLD for 2N-2N2P family

3.3. Pass transistor Adiabatic Logic (PAL) family

In PAL, the ground node of 2N2P is connected to power supply rail as shown in fig.7, in order to eliminate the non-adiabatic energy consumption. PAL achieves fully adiabatic operation at the cost of higher speed of operation. Cascaded PAL gates are controlled by two-phase clocks.

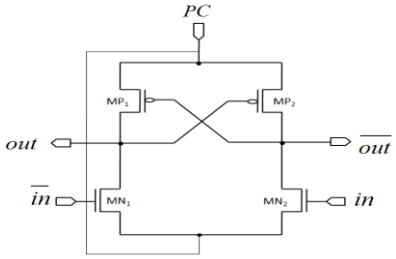

Fig.7. PAL buffer/inverter

Reliability logic diagram for the PAL family is as shown in fig.8.

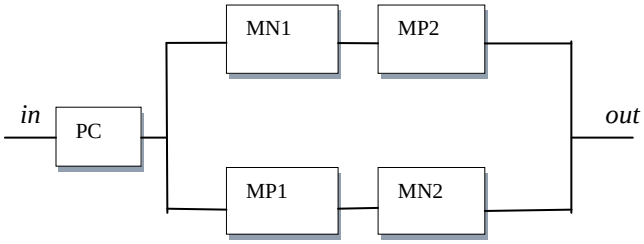

Fig.8. RLD for PAL family

3.4. Clocked CMOS Adiabatic Logic (CAL) logic family

Fig.9 shows an inverter designed in CAL, an adiabatic logic related to 2N-2N2P. The main structural difference between CAL and 2N-2N2P is the path control switches in the pull-down tree. In CAL, cascaded structures are controlled by a single-phase power-clock and two auxiliary square-wave clocks (c_x and *compliment* c_x).

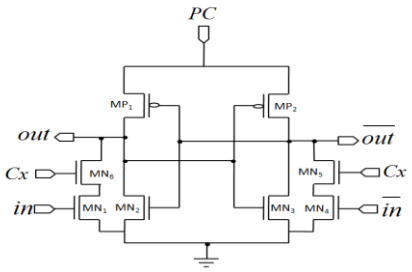

Fig.9. Inverter designed in CAL

Reliability logic diagram for the CAL family is as shown in fig.10.

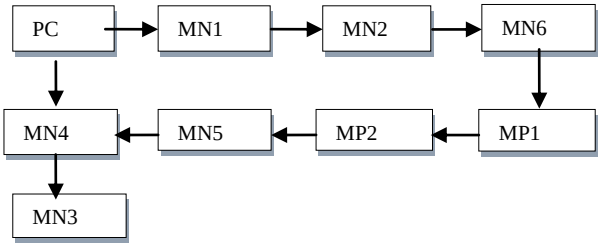

Fig.10. RLD for CAL family

3.5 Positive-Feedback Adiabatic Logic (PFAL) family

Among the MOSFET-only logic families, PFAL shows the best properties in the high frequency range. Fig.11 shows the general schematic of a PFAL gate. The input n-channel transistors evaluating the logic function F are connected between the oscillating power supply and the output nodes. The cross-coupled inverters (latch) drive the dual-rail encoded output signals (*out and compliment out*). The power clock supply PC has a phase shift of 90^o compared to the dual-rail encoded input signals *in* and *compliment in*. When the input signal *in* is low (compliment *in* is high), the output signal *out* follows the oscillating power clock supply PC where as compliment *out* stays at ground and vice versa.

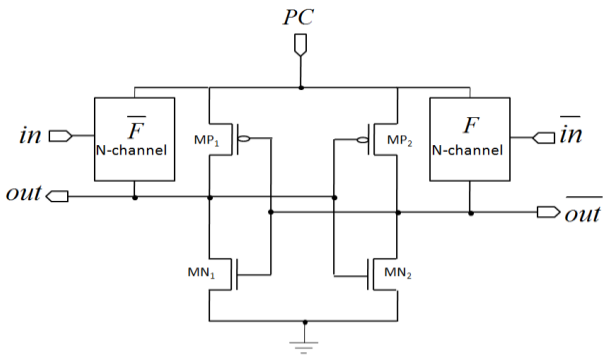

Fig.11. PFAL family

Reliability logic diagram for the PFAL family is as shown in fig.12.

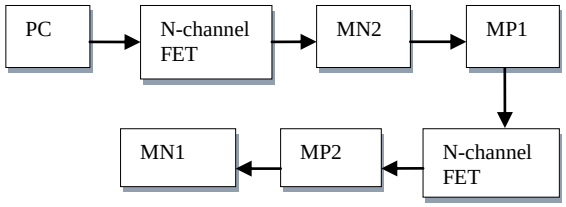

Fig.12. RLD for PFAL family

IV. FAILURE RATE AND RELIABILITY PREDICTION OF ADIABATIC LOGIC FAMILIES

A reliability prediction is a quantitative assessment of the level of reliability inherent in a design or achieved in a test model or production product. A well conducted reliability prediction also provides an awareness of potential equipment degradation during the equipment life cycle. Performing a reliability prediction provides visibility of equipment reliability requirements in the early development phase. The result of reliability prediction can be utilized to improve the equipment designs, to prevent the costly over-designs and to minimize the development testing time.

The prediction method shares several assumptions:

- During the useful life of a product, the failure rates of the individual components are constant.
- The failures of different components are considered statistically independent.
- The base failure rate for a component is its failure rate at a reference temperature and electrical stress. The base failure rate of a component is multiplied by thermal and electrical stress acceleration factors to find its failure rates in the product.
- The assembly reliability model is a series one – failure in any component causes an assembly failure.
- Only hardware failures were taken into consideration in the reliability prediction.

In this paper, we performed reliability prediction based on 'Parts count method' [8]. The components used in adiabatic logic families are power clock generator, NMOS, and PMOS. The Frequency of operation and model of each logic family [6] to which reliability prediction has carried out are listed in table I. failure rates of NMOS, PMOS, and PC at their maximum rated temperature levels are presented in table II, table III, and table IV respectively.

TABLE I
Frequrncy of Operation and Adiabatic Logic Family Model Used For Reliability Prediction

Logic style	Maximum operating frequency (in MHz)	Model
2N2P	100	Unknown power dissipation
2N-2N2P	100	Unknown power dissipation
PAL	100	Unknown power dissipation
CAL	100	Unknown power dissipation
PFAL	100	Unknown power dissipation
CMOS	100	Unknown power dissipation

TABLE II
Temperature Stress Levels and Failure Rate of Nmos in Each Adiabatic Logic Family

Component	Logic style	Temperature Stress levels		λ in FPMH
		Max	Min	
NMOS	2N2P	110	25	0.1701
NMOS	2N-2N2P	110	25	0.1701
NMOS	PAL	110	25	0.1701
NMOS	CAL	110	25	0.1701
NMOS	PFAL	110	25	0.1701

TABLE III
Temperature Stress Levels and Failure Rate of Pmos in Each Adiabatic Logic Family

Component	Logic style	Temperature Stress levels		λ in FPMH
		Max	Min	
PMOS	2N2P	110	25	0.1854
PMOS	2N-2N2P	110	25	0.1854
PMOS	PAL	110	25	0.1854
PMOS	CAL	110	25	0.1854

PMOS	PFAL	110	25	0.1854

TABLE IV
Failure Rate of Pc in Each Adiabatic Logic Family

Component	Logic style	λ in FPMH
PC	2N2P	0.0016
PC	2N-2N2P	0.0009
PC	PAL	0.0027
PC	CAL	0.0027
PC	PFAL	0.0009

Electronic components follow exponential distribution [7]. Therefore, by suitably adopting the mathematical forms for series, parallel, and series-parallel configurations given in [8] The net failure rate of each adiabatic logic family is as shown in table V.

TABLE V
Net Failure Rates of Adiabatic Lofic Families

S.No	Logic family	λ_{net} (per million hours)
1	2N2P	0.0138
2	2N-2N2P	1.0521
3	PAL	0.0149
4	CAL	1.8019
5	PFAL	1.0521
6	CMOS	0.3555

For exponential models, the reliability is given by [5]

$$R(t) = e^{-\lambda * t} \quad \ldots\ldots\ldots\ldots\ldots (2)$$

Where 'λ' is failure rate,' t ' is time of operation.

Following eq.2, the reliability of each logic family for 10^5 hours is evaluated and tabulated in table VI.

TABLE VI
Reliability of Each Adiabatic Logic Family for 10^5 Hours

S.No	Logic family	Reliability (for 10^5 hours)
1	2N2P	0.98632
2	2N-2N2P	0.90013
3	PAL	0.98521
4	CAL	0.83511
5	PFAL	0.90013
6	CMOS	0.96507

In this paper, we have compared the transistor adiabatic logic styles found in the literature and reported the results. All simulations are performed for inverter/buffer at the schematic level using a standard 0.18 µm CMOS technology. The performance and power dissipation of the logic styles are evaluated for a maximum frequency of operation of 100MHz. The results indicate that the PAL logic outperforms other adiabatic styles in terms of energy efficiency and complexity of structure. It also operates on only two clock phases. But PAL suffers from the floating output node problem during the charging phase. Also it is observed that the PAL logic does not function properly at lower frequencies. PFAL overcomes both of these drawbacks of PAL logic; however, it operates on four clock phases, which is a considerable overhead in practical system design. CAL logic can also be a good choice mainly because of its single clock operation. Fig.13 shows the comparison of power dissipation in various logic families.

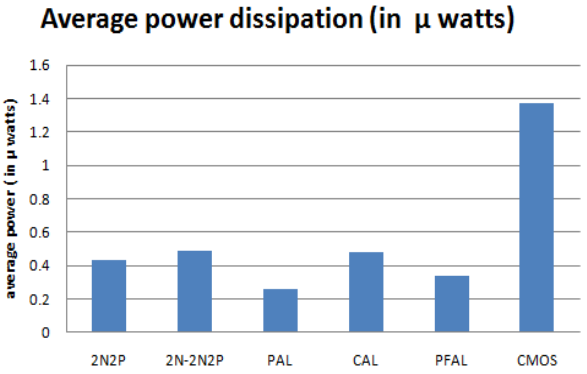

Fig.13. Comparison of power dissipation in adiabatic logic families

V. CONCLUSIONS

In this paper, we performed the reliability prediction analysis of each low power adiabatic logic families based on 'Parts count method'. From prediction data, we conclude that the 2N2P adiabatic logic family is highly reliable compared to other logic families considered. The result of reliability prediction analysis can be utilized to improve the equipment designs, to prevent the costly over-designs and to minimize the development testing time. Based on the reliability prediction, a designer has an important role in improving the logic families' reliability with effective design up gradations without change in their actual functionality. High reliable logic families are in high demand for applications such as: digital computers, laptops, cellular mobiles, and in any kind of portable electronic devices. This paper also attempted to find the best adiabatic logic family in terms of low power dissipation. Based on the simulation results obtained we conclude that PFAL is the best logic family for practical system design.

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AUTHOR PROFILE

Suresh Kumar Pittala received B. Tech degree in Electronics & Communication Engineering from RVR & JC College of Engineering, Guntur, A.P, India and M. Tech degree in Microelectronics and VLSI from National Institute of Technology Calicut, Kerala, India in 2005 and 2008 respectively. From 2008 till date he is working in the department of Electronics and Communication Engineering in DVR & Dr HS MIC College of Technology, Kanchikacherla, A.P, India. Presently he is pursuing Ph.D. from Acharya Nagarjuna University, Guntur, A.P, India. His research interests include Low Power VLSI Design, Analog and mixed signal VLSI Design and High Speed Interconnects.

Swajeeth Pilot. Panchangam is doing M.S (By Research) in Reliability Engineering Centre at Indian Institute of Technology, Kharagpur, India. He received B.Tech degree in Electronics and Communications Engineering. His research area of interest is Reliability modeling and performance analysis of sensor systems.

Dr. A. Jhansi Rani obtained her B. Tech Degree in Electronics and Communications Engineering from Velagapudi Ramakrishna Siddhartha Engineering College, Vijayawada, India in 1991 and M. Tech Degree in Microwave Engineering from Institute of Technology, Banaras Hindu University, Varanasi, U.P, India in 1993. Later she joined as a Faculty in ECE Dept., of V. R. Siddhartha Engineering College, Vijayawada, India. She obtained Ph.D. Degree from JNTU, Hyderabad, A.P, India in August 2008. She has about 36 technical publications in various International and National Journals and Conferences to her credit. She is the Life Member of FIETE, MISTE, BMESI, MSEMCEI. She received grants from DST and AICTE in the area of smart Antennas. Her fields of interest include Electro-magnetics, Smart Antennas, Analysis of Microwave Components, EM Waves and Transmission Lines, Numerical Methods and Applications and VLSI Design.