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Design and Implementation of DSSS-CDMA Transmitter and Receiver for Reconfigurable Links Using FPGA

R. Sarojini, Ch.Rambabu

Abstract- Direct sequence spread Spectrum (DSSS), is also called as direct sequence code division multiplexing (DS-CDMA). In direct sequence spread spectrum, the stream of information to be transmitted is divided into small pieces, each of which is allocated across to a frequency channel across the spectrum. A data signal at the point of transmission is combined with a higher data-rate bit sequence (also called chipping code) that divides the data according to a spreading ratio. The redundant chipping code helps the signal resist interference and also enables the original data to be recovered if data bits are damaged during the transmission. Direct sequence contrasts with the other spread spectrum process, known as frequency hopping spread spectrum. Frequency hopping code division multiple access (FH-CDMA), in which a broad slice of the bandwidth spectrum is divided into many possible broadcast frequencies. In general, frequency-hopping devices use, less power and are cheaper, but the performance of DS-CDMA systems is usually better and more reliable. In this project direct sequence spread spectrum principle based code division multiple access (CDMA) transmitter and receiver is implemented in VHDL for FPGA. The transmitter module mainly consists of data generator, programmable chip sequence generator (PN sequence generator), direct digital frequency synthesizer (DDFS), BPSK modulator blocks. The receiver modular mainly consists of BPSK demodulator, programmable chip sequence generator (PN sequence generator), matched filters, threshold detector blocks. Modelsim 6.2(MXE) tool will be used for functional and logic verification at each block. The Xilinx synthesis technology (XST) of Xilinx ISE 9.2i tool will be used for synthesis of transmitter and receiver on FPGA Spartan 3E.

Keywords: CDMA, DSSS, BPSK, PN code, DDFS.

I. INTRODUCTION

In communication systems an attractive approach for economical, spectral efficient, and high quality digital cellular and personal communication services is the use of Direct sequence code division multiple access (DS-CDMA) technique [1]. Due to its improved privacy and security, increased capacity.

VHDL implementation of DS-CDMA transmitter and receiver has been proposed in this project. Every mobile handset and every wireless base station operates on the same frequency spectrum .In order to discriminate one conversation from the other, every handset broadcast a unique code sequence is called as pseudo noise code. In this project pseudo noise code [3] is generated by using two six bit LFSRs. Code signal is called as chip signal. The chips modulated by the carrier using a digital modulation technique BPSK. The carrier is generated by using the technique discrete digital frequency synthesizer. CDMA base stations must be able to discriminate this different code sequences in order to distinguish one transmission from other. This discrimination is accomplished by means of a matched filter. A matched filter is a filter whose frequency spectrum is exactly designed to match the frequency spectrum of the input signal. Here matched filter generating the pseudo noise code, generated noise code is correlated with the received code and detecting original data.

In the recent years the CDMA on FPGA platform has attracted attention of academic research and industry. The Spartan TM-3E family of Field-Programmable Gate Arrays (FPGAs) is specifically broadband designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The five-member family offers densities ranging from 100,000 to 1.6 million system gates. Because of their exceptionally low cost, Spartan -3E FPGAs are ideally suited to a wide range of consumer electronics applications, including access, home networking, display/projection, and digital television equipment.

II. LITERATURE SURVEY

The cellular concept originated at Bell Labs in 1947. The first automatic analog cellular system started operation in Japan in 1979 and in the Nordic countries in 1981. The first commercial AMPS wireless cellular system in the United States started in October 1983 in Chicago. Analog cellular service operates on the 800 MHz frequency band, and are based on FDMA (Frequency Division Multiple Access). Within a few years after analog cellular systems were introduced in 1983, it became apparent that higher capacity, more reliable, and lower cost wireless systems were needed to meet booming demand. Predictions were made that system capacity would be saturated by the 1990's, first in the largest cities and then in other locations. When consumer demand saturates the capacity of a cellular system, there are three ways to expand: move into new spectrum bands, split existing cells into smaller cells, or introduce new technology to make more efficient use of existing bandwidth. Since no new radio spectrum would be available, and splitting cells requires very expensive additional network infrastructure especially in congested areas, new technology seemed to be the best route.

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* Correspondence Author
R. Sarojini, M.Tech. (DECS) student, GEC, Gudlavalleru
Ch. Rambabu, Assistant professor, GEC, Gudlavalleru

In 1988, a Cellular Technology Industry Association (CTIA) subcommittee was established in the United States to identify technology requirements. Cellular service operators and the manufacturing industry worked with CTIA to define a series of specific milestones to be achieved, with the goal of introducing new technology products and services by 1991.

The Telecommunications Industry Association (TIA) was asked to create a specification based on these requirements. Many proposals and much debate ensued, with major factions backing Time Division Multiple Access technology and others backing Frequency Division Multiple Access (FDMA). Both technologies evolved from the original AMPS. TDMA Interim Standard 54 (IS-54) was released in early 1991. TDMA equipment was demonstrated and tested in 1991 in Dallas and Sweden. Newer, more comprehensive standards have been released since, including TDMA IS-136 (also called Digital AMPS or D-AMPS), and CDMA IS-95, and the European GSM standard. Each of these has inherent advantages over AMPS technology.

III. MULTIPLE ACCESS TECHNIQUES

Multiple access schemes are used to allow many simultaneous users to use the same fixed bandwidth radio spectrum. In any radio system, the bandwidth that is allocated to it is always limited. For mobile phone systems the total bandwidth is typically 50 MHz, which is split in half to provide the forward and reverse links of the system. Sharing of the spectrum is required in order to increase the user capacity of any wireless network. FDMA, TDMA and CDMA are the three major methods of sharing the available bandwidth to multiple users in wireless system. Among these multiple access techniques CDMA provides less interfered and more secured type communication which is of more concern [3].

A. Frequency Division Multiple Access

For systems using Frequency Division Multiple Access, the available bandwidth is subdivided into a number of narrower band channels. Each user is allocated a unique frequency band in which to transmit and receive on. During a call, no other user can use the same frequency band. Each user is allocated a forward link channel (from the base station to the mobile phone) and a reverse channel (back to the base station), each being a single way link. The transmitted signal on each of the channels is continuous allowing analog transmissions. The channel bandwidth used in most FDMA systems is typically low (30 kHz) as each channel only needs to support a single user.

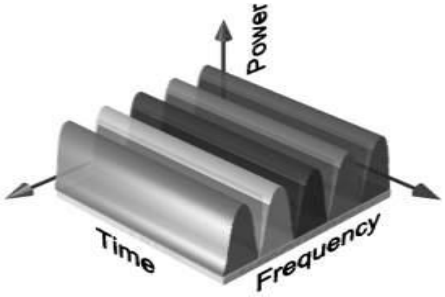

Fig.1. FDMA

B. Time Division Multiple Access

Time Division Multiple Access (TDMA) [16] divides the available spectrum into multiple time slots, by giving each user a time slot in which they can transmit or receive TDMA systems

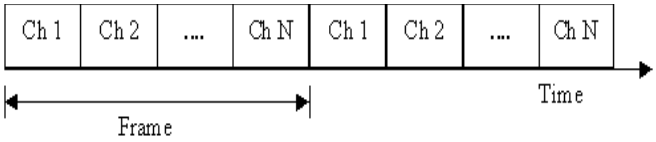

Fig.2. TDMA schemes where each user is allocated a small time slot

Transmit data in a buffer and burst method, thus the transmission of each channel is non-continuous. The input data to be transmitted is buffered over the previous frame and burst transmitted at a higher rate during the time slot for the channel. TDMA cannot send an analog signal directly due to the buffering required, thus is only used for transmitting.

C. Code Division Multiple Access

Code Division Multiple Access (CDMA) [3] is a spread spectrum technique that uses neither frequency channels nor time slots. With CDMA, the narrow band message (typically digitized voice data) is multiplied by a large bandwidth signal that is a pseudo random noise code (PN code). All users in a CDMA system use the same frequency band and transmit simultaneously. The transmitted signal is recovered by correlating the received signal with the PN code used by the transmitter.

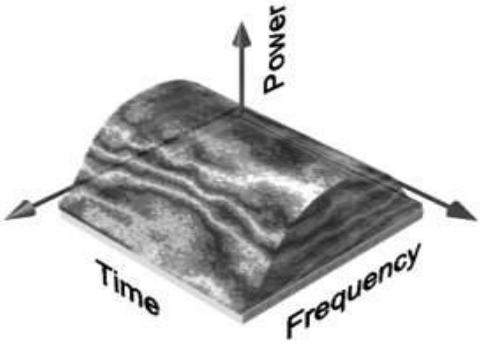

Fig.3. Code division multiple Access (CDMA)

CDMA technology was originally developed by the military during World War II. Researchers were spurred into looking at ways of communicating that would be secure and work in the presence of jamming. Some of the properties that have made CDMA useful are:

- Anti-jam and interference rejection
- Information security
- Accurate Ranging

IV. SPREAD SPECTRUM TECHNIQUES

- Frequency hopping spread spectrum
- Direct sequence spread spectrum

A. Frequency Hopping Spread Spectrum

The signal is broadcasted over a random series of radio frequencies, hopping from one frequency to another frequency at fixed intervals a receiver, hopping between frequencies in synchronization with the transmitter picks up the message

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B. Direct Sequence Spread Spectrum

Each bit in the original signal is represented by multiple bits in the transmitted signal, using a spreading code [9]. The spreading code spreads the signal across a wider frequency band in direct proportion to the number of bits used

C. Direct Sequence CDMA Generation

DS-CDMA [5] is achieved by spreading the data signal by a pseudo random noise sequence (PN code), which has a chip rate higher than the bit rate of the data. The PN code sequence is a sequence of ones and zeros (called chips), which alternate in a random fashion. The PN code used to spread the data can be of two main types. A short PN code (typically 10-128 chips in length) can be used to modulate each data bit. The short PN code is then repeated for every data bit allowing for quick and simple synchronization of the receiver. Alternatively a long PN code can be used.

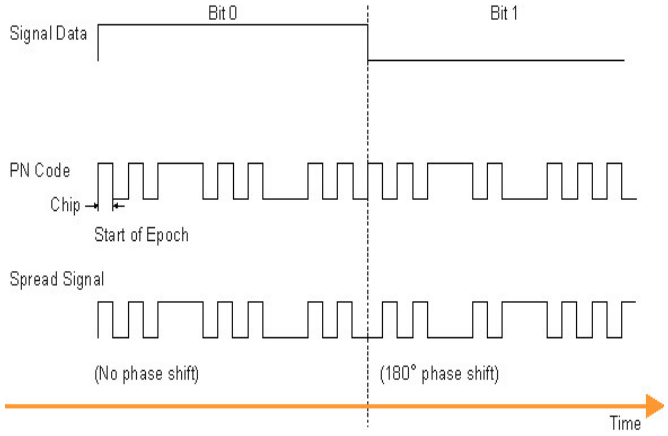

Fig.4. Direct sequence signals

In DS-CDMA the spreaded signal is modulated by a RF carrier. For the modulation, various modulation techniques can be used, but usually some form of phase shift keying (PSK) like binary phase shift keying (BPSK), differential binary phase shift keying (D-BPSK), quadrature phase shift keying (QPSK), or minimum shift keying (MSK) is employed.

V. HARDWARE AND SOFTWARE DESIGN AND IMPLEMENTATION

A. Specifications Being Considered For Design

1. Type of PN Sequence: Gold Code
2. LFSR Size: Two 7 bit LFSRs in case of Gold Sequence
3. PN Sequence Length: 127 in case of gold sequence
4. Maximum no. of communication Links: 63 in case of gold sequence 5.Type of Modulation : BPSK
6. Type of demodulation : Coherent BPSK demodulation
7. Type of Correlator : Matched Filter
8. Type of Signal Synthesis: LUT based direct digital fequency

Synthesis

9. Phase Resolution Chosen in DDFS : 5.625°
10. Threshold Type adjustable: Constant Threshold value
11. Front end Design Entry : VHDL
12. Backed Synthesis : Xilinx Spartan 3E FPGA

Following tools are used while developing, testing, implementing and programming the CDMA transmitter and receiver blocks.

Simulation - Modelsim Xilinx Edition (MXE)

Synthesis - Xilinx Synthesis Technology (XST) of Xilinx ISE

B. CDMA Transmitter

In CDMA transmission user data is spreaded by a PN sequence and then modulated using BPSK modulation where in the carrier is generated using digital frequency synthesizer principle .Then the modulated signals from different users are combined and transmitted.

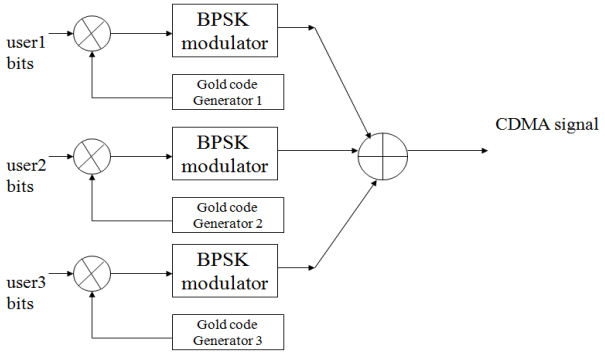

Fig.5. Block diagram of multiple user CDMA transmitters

The main blocks of CDMA transmitter are listed below.

- Clock distributor
- PN sequence generator
- Signal spreader
- BPSK modulator

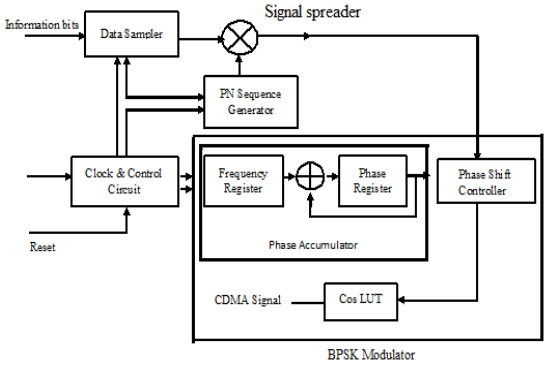

Fig.6. Block diagram of CDMA transmitter.

A. Clock Distributor

The clock distributor of CDMA transmitter derives different clock signals from master clock, which are required for Spread spectrum signal generation.

B. PN Sequence Generation

The important block of DS-CDMA communication system is the PN sequence generator. The PN sequence generator can be implemented using LFSR's to generate several types of PN sequences. Two types of PN sequence generators implemented in this project. They are ML sequences and gold codes

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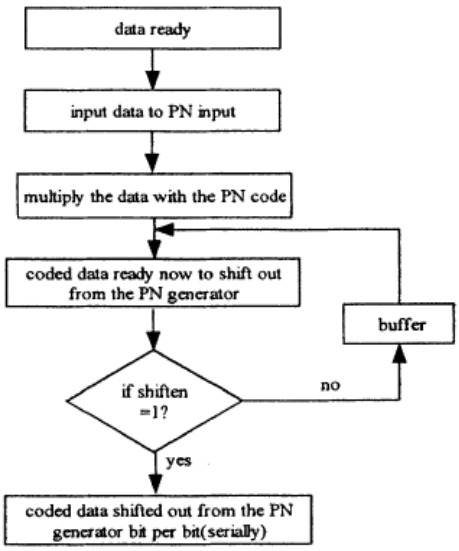

Fig.7. the flow chart of the PN generator

Maximal length sequence are LFSR based PN sequence generators which can produce the maximum possible length sequence. For n bit size shift registers the PN sequence length will be 2^n-1 bits. In this case 6 bit LFSR is implemented. Length of ml sequence generated is 63.Number of communication links that can be supported is 63.

C. Gold Sequence Generator:

The length of the Gold Sequence is 2^n-1

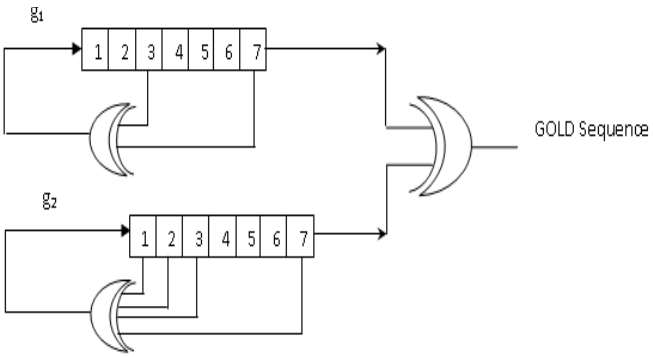

Fig.8. Gold Sequence Generator.

Length of gold sequence generated is 127 Number of communication links supported is a 63.Correlation property of gold sequences is better than ml sequences and hence they are more preferred.

D. Signal Spreader

The function of signal spreader is to generate PN sequence when the information bit is '1' and generate the complement of the PN sequence if the information bit is '0'. The digital implementation of signal spreader is achieved by using XOR gate controlled inverter action. The spreaded chip signal is used for modulation by BPSK modulator.

E. BPSK Modulator

The BPSK modulator produces the band pass spread spectrum signal which is suitable for transmission from the spreaded signal. The BPSK modulator is implemented using pure digital architecture. The Direct Digital Frequency Synthesis (DDFS) technique with phase shifting provision is used for the signal generation.

C. DS-CDMA Receiver

The CDMA receiver gets its input from the transmitter section and recovers the data using matched filter. The matched filter can distinguish the PN sequence and the passes the data to the respective user.

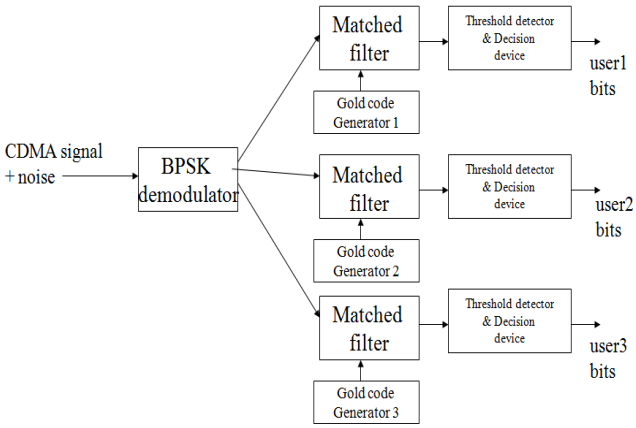

Fig.9. Block diagram of multiple user CDMA receivers.

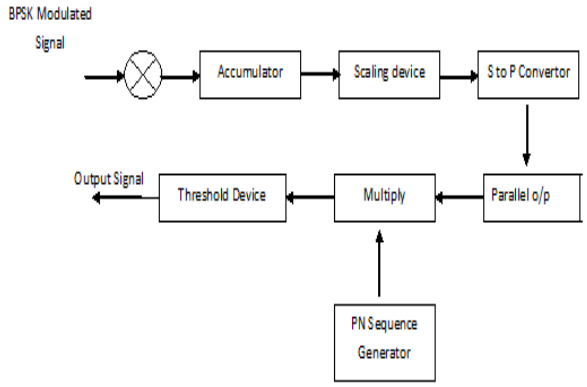

Fig.10. CDMA Receiver

The receiver performs the following steps to extract the Information:

- Demodulation
- Accumulation
- Scaling
- Serial to parallel conversion
- Multiplying and dispreading
- Threshold device

A. BPSK Demodulator

BPSK demodulator principle is used in this project for receiving the DS-CDMA signals. The BPSK demodulator produce 15 (-7 to 7) digital words, unlike in conventional BPSK demodulator which produces only two symbols ('1' and '0'). This is necessary due to the low power spectral density of DS-CDMA signals and it is only possible to detect the information bits after correlation.

B. Multiplier

A signed multiplier is used to multiply the incoming signal with the LO output. The multiplication is performed in 2's complement and the 15 bit result is given to the accumulator.

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C. Local oscillator

The Local oscillator produces 6 bit signed bits representing the COS signal. The same principle DDFS which is used in transmitter is used in the receiver.

D. Accumulator

The accumulator in the receiver corresponds to the integrator in the analog equivalent. The accumulator accumulates the outputs of multiplier for one symbol duration and outputs at the beginning of next symbol.

E. Scaling device

The scaling device accepts the output of accumulator and scales its value to 4 bit signed number range, i.e., -7 to +7. This is done in order to reduce the complexity at the correlator and even at the hardware implementation level.

F. Serial to parallel converter

The serial to parallel converter accepts the outputs of the BPSK demodulator and produces parallel vector with an array of 128 words. This parallel 128 words constitute the most recent 128 outputs of the BPSK demodulator. This becomes input to the correlator.

G. PN sequence generator

The PN sequence generator is same as the one cussed in transmitter, except in the output type. In the transmitter side the output of PN sequence generator continuously produces PN sequence on one bit output. But in the receiver side, since the complete PN sequence is required every time for correlating with the outputs of BPSK demodulator it is provided as a parallel vector. Another difference is the '1' of PN sequence is provided as +1 and '0' is provided as -1, which is the required form for correlator.

H. Matched filter

Matched filter based correlator is used in this project for receiving the DS-CDMA signals. The correlator accepts the 128 demodulator outputs and multiplies with 128 length PN sequence which is a sequence of +1 and -1. The outputs of multipliers are accumulated to produce the correlator output. The magnitude of the correlator output peaks whenever exact match occurs between the PN sequence and BPSK demodulator outputs. The output of the matched filter is given to the threshold detector, for detecting the information bits.

I. Threshold detector

The threshold detector compares the magnitude of the correlator output with the threshold value. If the magnitude of the correlator output is higher than the threshold value, then it raises a flag indicating that one bit is detected. If the sign of the correlator output is positive, then it will be interpreted as '1'. Otherwise it will be declared as '0'. This is the detected information bit.

VI. RESULTS

A. Simulation Results

a. Simulation result for DS CDMA Top level module

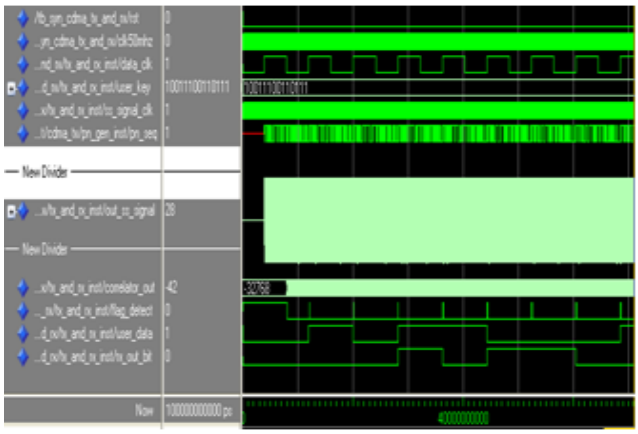

Fig.11. Simulation result for DS CDMA top level module

The above simulation result shows the top level module DS CDMA transmitter and receiver. It can be observed that the received data is same as user data with some amount of delay.

- user key of 14 bits is applied to generate 127 bit gold sequence
- Buf_data – It is the user data which is sent to the spreader after buffering so as to maintain synchronization
- PN_seq – It is the generated 127 bit gold sequence which is used for spreading
- Sos- it indicates the start of PN-sequence when it is 1
- Chip_signal – It is the signal obtained after spreading and is same as PN_sequence if the buf_data is 1 else it is complement of the pn_sequence
- Out_ss_signal – It is the transmitted DS CDMA signal
- Correlator_out – It is the output of correlator
- Flag_detect – It is raised to 1 whenever a bit is detected. A bit is detected when the correlator output is greater than threshold value.

B. Chipscope Analysis Results

a. Chip Scope pro analyzer DSCDMA Top level Module

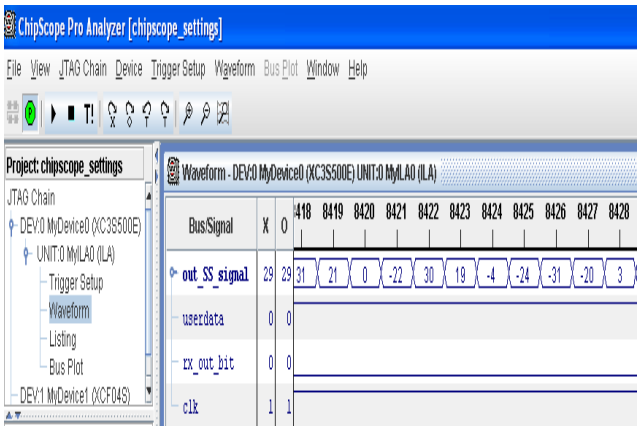

Fig.13. chipscope pro analyzer DS CDMA top level module

The above chipscope pro analyzer output shows the transmitted signal which is out_ss_signal. It can be observed that user data bit and rx_out_bit user are equal.

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C. Synthesis Results

A. DS CDMA transmitter and receiver Final Report

RTL Top Level Output File Name : syn_CDMA_tx_and_rx.ngr
Top Level Output File Name : syn_CDMA_tx_and_rx
Output Format : NGC
Optimization Goal : Speed
Design Statistics
IOs: 40
Device utilization summary:
Selected Device : 3s500efg320-5
Number of Slices: 1542 out of 4656 33%
Number of Slice Flip Flops: 821 out of 9312 8%
Number of 4 input LUTs: 2545 out of 9312 27%
Number of bonded IOBs: 38 out of 232 16%
IOB Flip Flops: 2
Number of MULT18X18SIOs : 1 out of 20 5%
Number of GCLKs: 3 out of 24 12%
Timing Summary:
Speed Grade : -5
Minimum period: 129.116ns (Maximum Frequency: 7.745MHz)
Minimum input arrival time before clock: 9.552ns
Maximum output required time after clock: 12.392ns
Maximum combinational path delay: No path found.

B. Floor plan for CDMA top block

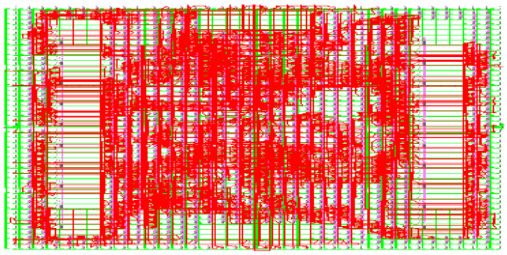

Fig.14. Floor plan for CDMA top block

The Floor plan for CDMA top block on Spartan-3E FPGA is given in the above figure.

C. DS CDMA Top Level RTL Schematic

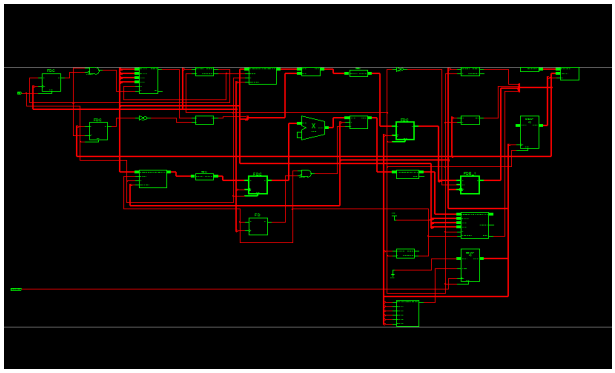

Fig.15. DS CDMA Top Level RTL Schematic

VII. CONCLUSION

In the proposed Project I have implemented various modules of Direct Sequence Code Multiple Access Communication System. It has been observed that the implemented design is fully reconfigurable on any communication links. System developed is implemented with 127 gold code sequence, it can be implemented with any length sequence very easily.

The developed DS CDMA system provides efficient area utilization on FPGA. This is obtained by implementing scaling process in receiver section. Chipscope analysis which provides testing and on chip debug at runtime is also implemented and the results obtained are satisfactory.

FUTURE SCOPE

The proposed project can be further extended to implement with multiple transmitters and receivers .It can be implemented with different modulation techniques and a comparative analysis can also be made. Various techniques can also be implemented to improve the multipath interference effect.

The concept can be extended to design the Global Positioning System which is CDMA system. Frequency hopping spread spectrum technique can also be implemented and compared.

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AUTHOR PROFILE

Ms. R.Sarojini, obtained her B.Tech degree from Shri Vishnu Engineering College for Women, affiliated to JNTU Kakinada, Bhimavaram, west Godavari district, Andhra Pradesh, India in the year 2010. Now she is pursing M.Tech degree from Gudlavalleru Engineering College, Gudlavalleru, affiliated to JNTU Kakinada, Krishna district, Andhra Pradesh, India. she participated in workshops. She is interested in the field of communications and image processing.

Mr. Ch.Rambabu, obtained his B.Tech degree from V.R.Siddhardha Engineering College, Kanuru, Vijayawada, Krishna District, Andhra Pradesh, India. And he obtained his M.Tech degree in Gudlavalleru Engineering College, affiliated to JNTU Kakinada,, Gudlavalleru, Krishna district, Andhra Pradesh, India. He is having 5 years experience in the field of wireless communications and embedded systems.

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