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# Design and Construction of Single Phase Cycloconverter

**Rajib Baran Roy, Md. Ruhul Amin**

***Abstract*: The variable frequency has always been of great importance in the industrial world. The generating station generates electricity of the frequency of 50 Hz which is not always applicable for some electrical appliances. Some electrical devices need variable frequency ranging from one tenth to one third of the supply frequency. Some examples are induction motors used in AC traction, aircraft power supplies, mobile power supplies and others. Therefore the variable frequency generation becomes necessary for meeting the ever growing demand of industrial application. The cyclo-converter is such a device which generates variable frequency. The development of the semiconductor devices has made it possible to control the frequency of the cycloconverter according to the requirement and deliver a large amount of controlled power with the help of semiconductor switching devices like thyristors and others. The aim of this project is to design and construct a single phase cyclo-converter circuit which could generate variable frequency. The proper generation of the blanking and gate pulses of the switching devices and synchronizing them with the input signal is the most important thing in designing a cyclo-converter circuit which becomes easier due to the availability of the integrated circuit(IC). The use of 555 timer and operational amplifier ICs has simplified the generation of blanking and triggering signals. Moreover the synchronization of these signals with the input signal is performed by means of the comparator circuit where the operational amplifier IC is used. Due to the cost constraint, a transformer of secondary rating of 9V and 800mA is considered for designing the cycloconverter which delivers a power of about 7 W. This similar circuit can be used for large scale output power after some modifications in the control circuit. The cycloconverter circuit is designed as a prototype and the aspects of the commercial cycloconverter are not considered.***

***Index Terms:* cycloconverter,intergrated cicuit synchronization, variable frequency generation, prototype.**

## I. INTRODUCTION

The cyclo-converter is basically ac to ac power converters where the alternating voltage at supply frequency is converted directly to a lower frequency without going through any intermediate dc power conversion stage.

The cyclo-converter is traditionally used only in very high power applications usually above one megawatt.

Because of technical and economical reasons the cyclo-converter was not very popular for commercial use. The advent of the high power thyristor has revived the interest of the cyclo-converter circuits [1].

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The cyclo-converter is generally used for the speed control of motors, constant frequency power supplies, controllable reactive power supply for an ac system and induction heating system, VSCF (variable frequency input and constant frequency output) generation which is used in aircraft power suppliers, mobile power supplies and space vehicles. Since in induction and synchronous motors the speed is directly proportional to the supply frequency, the speed can be effectively controlled by controlling the input frequency. Generally the cycloconverter lies in the category of static frequency changer. Both three phase and single phase cycloconverters are used in different applications. The output frequency of a three-phase cycloconverter must be less than about one-third to one-half of the input frequency [1], [2], [11].

The cyclo-converter requires high power switching mechanism which is generally performed by thyristors, MosFETs and TRIACs in order to get alternating output of variable frequency. The quality of the output waveform improves if more switching devices are used. In case of high output power cyclo-converters of the range of a few megawatts, silicon-controlled rectifiers (SCRs) are used. However low-power cycloconverters, TRIACs are generally used for switching devices in place of SCRs. The advantage of using TRIAC is that it conducts in either direction of operation. It may be noted that the use of a cycloconverter is not as common as that of an inverter and it is used mostly in very high power applications [2].

## II. SINGLE PHASE CYCLO-CONVERTER

The cyclo-converter generally consists of two converter group one of which is called the positive converter and another one is negative converter. Generally the switching device of positive converter group goes in conduction during positive half cycle whereas the negative converter group goes in conduction during negative half cycle of the input wave shape[3]. The control circuit controls the operation of each converter group and provides synchronization of the output signal with the input signal. The basic circuit diagram of a single phase cyclo-converter is shown in the figure 1. The single phase cycloconverter is a 2 pulse cyclo-converter because there are two phase controlled pulses per cycle of the output phase [4].


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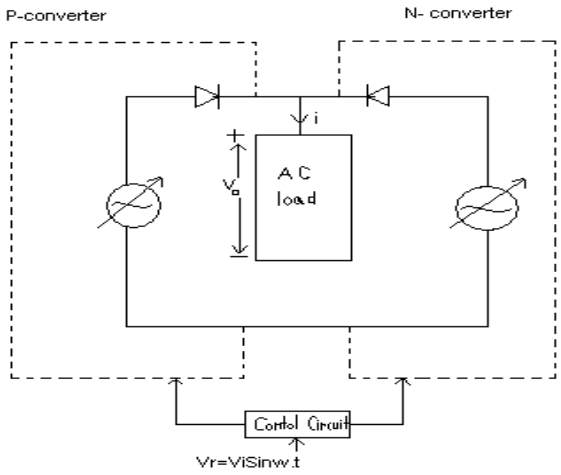


**Fig. 1 Basic Diagram of Single Phase Cycloconverter**

Generally the transformer is used for providing alternating output to the load and if a neutral return is not required in a multiphase output application, the transformer can be removed to simplify the circuit. The cycloconverter has four thyristors divided into a positive and negative bank of two thyristors each. The output voltage is controlled by phase control of the positive and negative bank thyristors in accordance with the flow of positive and negative current in the load respectively[1]. There are two groups of converter which can be defined as P and N. The P and N converters control the positive and negative half cycles of the output voltage of the desired frequency respectively which is shown in the figure 2. The conduction intervals of P and N converters are also marked in figure 2.

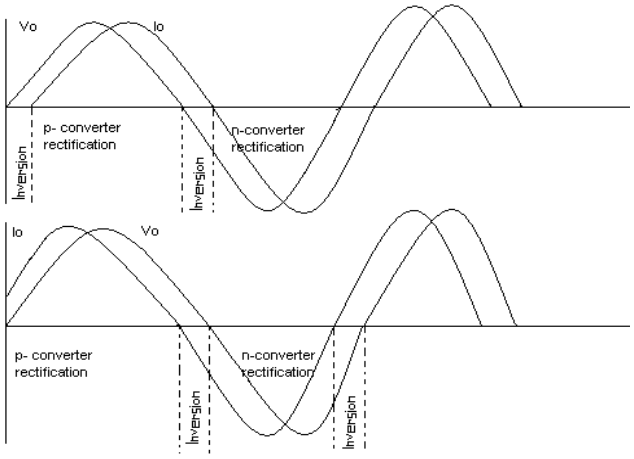


**Fig 2. Output Voltage and Current Waveforms of the Single Phase Cycloconverter**

The positive converter operates whenever the load current is positive with the negative converter remaining idle during this period. In a similar manner, the negative load current is supplied by the negative converter with the positive converter remaining idle during this period [3]. A cycloconverter circuit is comprised of power, control and filter sections.

### *A. Power Section of Cycloconverter Circuit*

The power section of cycloconverter comprises of a dual converter in which two groups of controlled rectifiers (thyristors) employ a common centre tapped transformer as their source[5]. Figure 3 shows the power section of a single phase cyclo-converter.

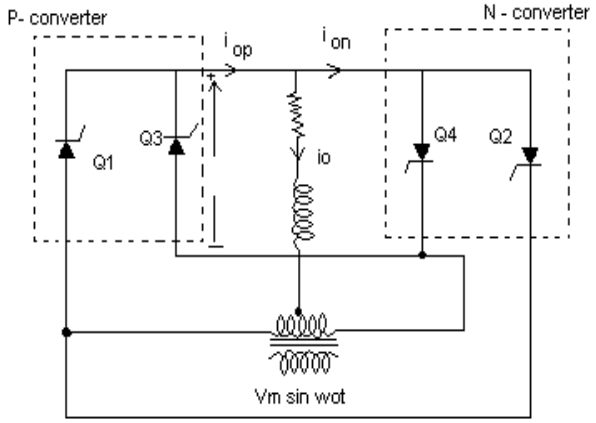


**Fig. 3 Power Section of Single Phase Cycloconverter**

The transformer can be replaced by its equivalent and further equivalent circuit is shown in figure 4. The $Q_1$ and $Q_3$ thyristors comprise the positive P converter group whereas the thyristors $Q_2$ and $Q_4$ comprise the negative Q converter group. The positive and negative load current is obtained from the conduction of $Q_1$ and $Q_3$ of the P converter and $Q_2$ and $Q_4$ of the Q converter respectively. The control circuit should be designed in such a way that the P converter goes in conduction during the positive half cycle of the input signal when the Q converter remains idle. Similarly when the Q converter goes in conduction during negative half cycle of the input signal the P converter remains idle. Two blanking signals P and N determine the operation of the thyristors in each converter group according to the sequence of the gate trigger. Moreover the frequency of the output signal depends on the frequency of the P and N blanking signals [6].

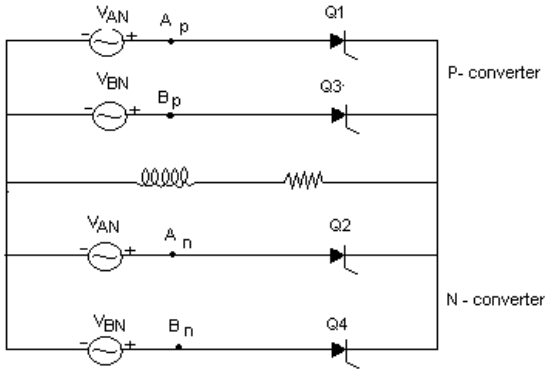


**Figure 4: Simplified Power Circuit of the Single Phase Cycloconverter**

The natural or line commutation is employed to turn off any conducting thyristor. The thyristors of any particular group go in conduction according to the sequence of the gate trigger. By turning on a thyristor in a particular group, a reverse voltage appears across the thyristor which was in conduction before that thyristor in the same group and thus the natural commutation of thyristors occurs sequentially[7],[8]. So by turning on the thyristor $Q_1$ of the positive converter group, the thyristor $Q_3$ gets commutated and vice versa.


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The commutation of the thyristors in the negative converter group occurs similarly. In case of the natural commutation, the current through a thyristor goes to zero before the incoming thyristor is turned on [6]. The thyristors $Q_1$ and $Q_4$ or $Q_2$ and $Q_3$ cannot be turned on simultaneously because this causes the short circuiting of the secondary voltage sources $V_{an}$ and $V_{bn}$ or the secondary winding of the transformer. When the load current is to be reversed from a positive value to a negative value, a changeover should take place from $Q_1$ to $Q_2$ or $Q_3$ to $Q_4$.

The gate triggers are applied to the P group thyristors whenever the blanking signal P is present and similarly the gate triggers are applied to the N group thyristors whenever the blanking signal N is present. The use of the centre tapped transformer provides two supplies which are shifted 180 degrees in phase with each other. When $V_{an}$ is positive, then the voltage at the anode of the thyristor $Q_1$ is positive and that at cathode is negative and similar situation occurs across the anode and cathode of the thyristor $Q_2$. This means that both $Q_1$ and $Q_2$ thyristors are ready to conduct if they are triggered at their gate. Since the conduction of thyristors is controlled by the application of blanking pulses and the gate triggering pulses so the triggering pulses are allowed to trigger the gates if and only if there are blanking pulses. The condition can be fulfilled by using the AND logic gate. However during conduction, the anode to cathode voltage, $V_{AK}$ of each thyristor is retained less than the breakdown voltage, $V_{BO}$ and therefore the rate of change of voltage, dv/dt needs to be less than the breakdown rate. The thyristor $Q_1$ of the P converter conducts only in the presence of both the P blanking pulse and the corresponding gate pulse $ig_1$.So the current first flows through the thyristor $Q_1$ and then through the load. Similarly the thyristor $Q_2$ of the N converter goes in conduction only in the presence of both the N blanking pulse and the corresponding gate pulse $ig_2$. In this case the current first flows through the load and then through the thyristor $Q_2$. The direction of the current through the load reverses in the latter case and hence the positive and the negative portion of the output wave can be obtained [8].

Similarly the thyristor $Q_3$ goes in conduction in the presence of both the P blanking signal and the corresponding gate pulse $ig_3$ and therefore the current first goes through the thyristor $Q_3$ and then through the load. The conduction of the thyristor $Q_4$ occurs in the presence of both the N blanking signal and the corresponding gate pulse $ig_4$ and in that case the current will go through the load first and then through the thyristor $Q_4$. The duration of the positive and negative portion of the output wave depends on the pulse width of the P and N blanking signals respectively. So the output frequency depends on the frequency of the blanking pluses and therefore it is necessary to have the same frequency of both the P and N blanking pulses. The sinusoidal output from the cycloconverter can be generated by using filter. For the inductive load, the cycloconverter needs to be carefully designed since the current doesn't zero when the input becomes zero [1]-[6].

### *B. Control Circuit*

The main function of the control circuit is to produce trigger pulses in a particular sequence and feed them to the gates of the positive and negative group of thyristors so as to generate a voltage of desired wave shape at the output terminals of a cycloconverter. The control circuit can be arranged broadly into four functional blocks which are (a) synchronizing circuit, (b) comparator circuit and reference voltage source, (c) converter group selection circuit and (d) logic and triggering circuit. The function of the synchronizing circuit is to generate low voltage signals to the control circuit. These low voltage signals need to be synchronized with the voltage supplied to the main power circuit. The step down transformer can be used with suitable filter circuit for this purpose for avoiding waveform distortion. The possible phase shifting circuit may also be required accordingly. The easiest method of achieving the synchronization of the low voltage signals with the voltages supplied to the main power circuit can be constructed by the use of the operational amplifier (OPAM 741). Since the thyristor should be triggered by the pulses which have the duration just greater than on time therefore the gate triggering of the thyristor by the above generated pulses is unfeasible. If the above square waveforms are used for gate triggering of the thyristor then huge power dissipation can be destructive for the thyristor and the negative pulses cause the thyristor to the false triggering. This difficulty can be eliminated by using the differentiator circuit which gives narrow spikes for thyristor gate triggering. The differentiator circuit and its output are shown in the figures 5(a) and 5(b) respectively [6], [11].

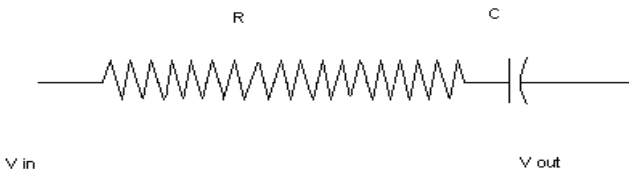


Fig. 5 (a) Differentiator Circuit

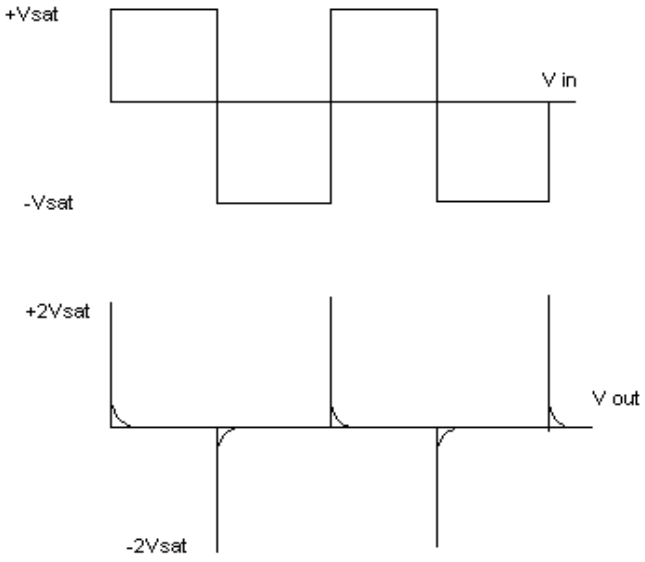


**Fig. 5 (b) Output of Differentiator Circuit**

This spike is used to trigger the monostable multivibrator. The configuration of the monostable multivibrator is shown in figure 6.


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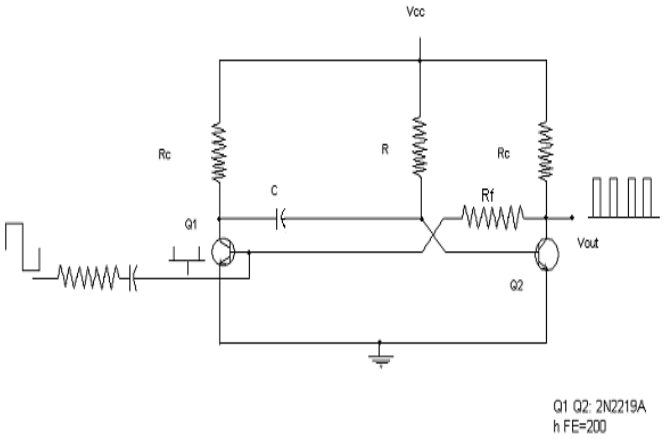


**Fig. 6 Monostable Multivibrator**

By adjusting the RC time constant of the multivibrator it is possible to obtain the output pulse (only positive) of any time period with the frequency half of the triggering spikes. The output of the monostable multivibrator is arranged in such a way that initially it is at low value. When the positive spike occurs at the base of the transistor, Q1 then that transistor goes into conduction. Its collector current increases and thereby its collector to emitter voltage decreases to a low value. Since the capacitor can't change the voltage across it instantaneously the whole abrupt change appears at the base of the transistor $Q_2$ and it remains at cutoff. Then its collector current becomes low and the collector to emitter voltage becomes high which drives the output of the multivibrator to a high value and the output remains at that value until the time period determined by RC time constant elapses. The output will remain in that stable state until the next spike pulse appears. The feedback resistor, $R_f$ gives the regenerative action thus lowering the transition time. So, when the transistor,$Q_1$ will be in saturation state then the transistor, $Q_2$ will be in cutoff state and vice versa[1],[4],[6].

Since the output pulse of the monostable multivibrator is the trigger pulse therefore the time period of the output pulse should be longer than the turn on time of the selected thyristor. Generally the turn on time of the thyristor is within the range of 150 to 200 µsec. In this case the RC time constant is considered of 220 µsec by selecting C = .022uf, R = 10kΩ, $R_f$ =10kΩ and Rc=1kΩ. The transistors (Q1, Q2) are of 2N 2219A type whose $h_{FE}$=200 and $V_{cc}$=15v. So by using the combination of the differentiator circuit and the monostable multivibrator, the positive pulse of the duration 220 µsec is obtained. These pulses are properly synchronized with the input signal. The overall output is shown the figure 7. In practical the output pulses lag the input signal which is desired in this case. Since the discontinuous current is required for natural commutation of the thyristor and the delay will perfectly serve the purpose. Thus the generation of the signals $i_{G1}$, $i_{G4}$ (non-inverting pulse) and $i_{G2}$, $i_{G3}$ (inverting pulse) is accomplished [1]-[5].

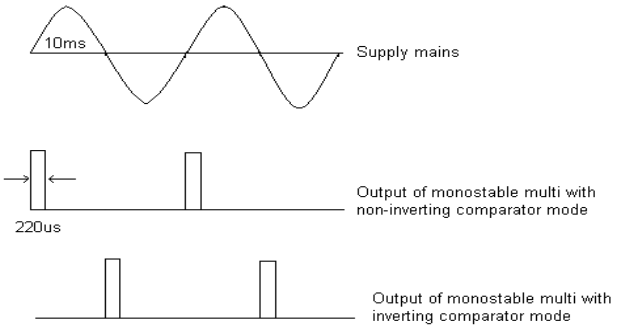


**Figure 7: Synchronized Output of Monostable Multivibrator**

For converter group selection, two blanking pluses are required and the blanking pluses are such that they have lower on time and higher off time. Moreover there is an $180^0$ phase displacement among them. Generally signals of higher on time and lower off time are generated and then inverting those signals the desired blanking signals can be obtained [6]. The 555 timer is used for generating these signals. The blanking signals, output of the 555 timer and not gate are shown in the figures 8(a), 8(b) and 8(c) respectively.

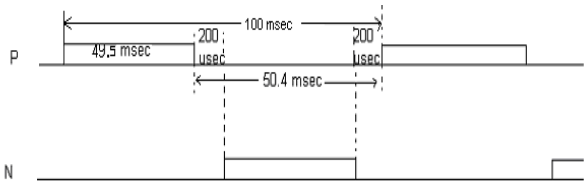


**Fig. 8 (a) P and N Blanking Signals**

**Fig. 8 (b) Output of the 555 Timer**

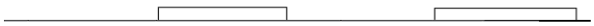

**Fig. 8 (c) Output of Not Gate**

The 555 timer can also be used as a clock pulse generator. Generally when it is used as an astable multivibrator which is shown in the figure 9 produces a series of rectangular output pulses. The two external resistors ($R_A$ and $R_B$) and a capacitor(C) are shown in the figure and the control voltage input (at pin 5) is usually left open which is not shown in this figure. But connecting a decoupling capacitor between the pin 5 and ground may improve the functional operation of the circuit. When the trigger input is less than 1/3Vcc, that comparator has a high output, setting the RS flip-flop. Then the Q output from the flip flop is low which is inverted to produce a high output signal from the 555 timer. When the threshold voltage exceeds 2/3 Vcc, the RS flip flop is reset which results in a high Q level and a low output signal from the timer. Whenever the Q output of the RS flip-flop is high, the transistor Q1 turned on. The transistor provides a low and high impedance path when it is turned on and off respectively. The reset input resets the status of the previous output of the flip-flop.



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It forces the Q signal of the flip flop to go high which produces a low output (after inversion) and thereby the discharge transistor is also turned on [8].

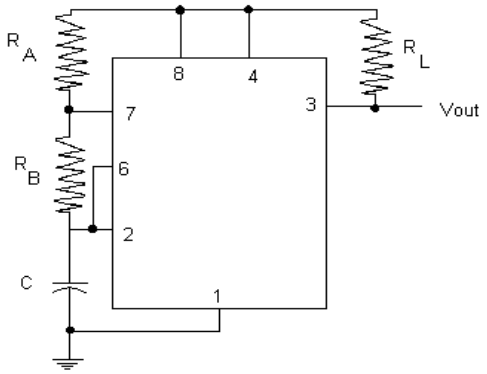



**Fig. 9 Astable Multivibrator by Using 555 Timer**

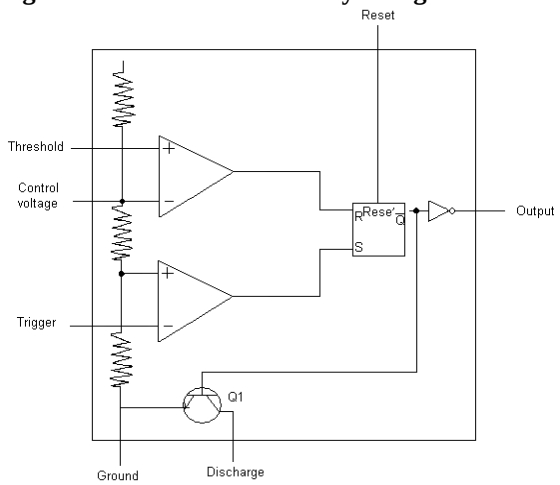



**Fig. 10 Internal Circuity of 555 Timer**

If the output signal of the figure 10 is initially high then the discharge transistor $Q_1$ is off. The capacitor charges up to Vcc through the resistors, $R_A$ and $R_B$ and the current are limited by these resistors**.** When the voltage of the capacitor reaches 2/3 of Vcc, the threshold comparator switches its output to the high level and the flip flop is reset. The Q becomes high and the output becomes low. The discharge transistor $Q_1$ is turned on and creates a ground at pin 7 of the timer [9]. Then the capacitor starts to discharge to the ground through $R_B$ until the voltage falls to the reference voltage on the trigger comparator. The trigger comparator then produces a high output and sets the flip flop. So the Q becomes low and the output of the timer becomes high and thereby the transistor Q1 turns off. The capacitor can once again charge through the two resistors, $R_A$ and $R_B$ and the cycle repeats [10].

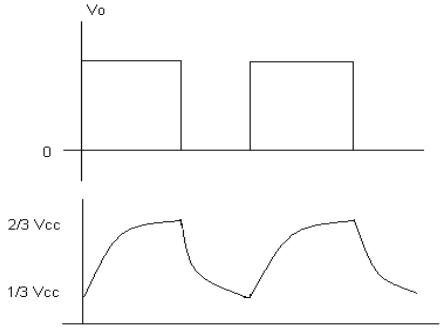



**Fig. 11 Timing Diagrams of the Stable Multivibrator**

The output voltage of the timer and the variation of the capacitor are shown in the figure 11. The capacitor voltage is clamped and varies between 1/3 to 2/3 Vcc. When the capacitor voltage reaches the upper extreme limit (2/3 Vcc) then the output voltage,Vo falls to 0 volt. Similarly when the capacitor discharges to the lower limit (1/3 Vcc) then output voltage,Vo again becomes high. If a dc power supply voltage of 5 volt is used then all the inputs and outputs of the timer are TTL compatible. The high and low time period of the output waveform can be determined by the following relationship.

For high output period:

$2/3\ Vcc = 1/3\ Vcc\ e^{t_H/(R_A+R_B)C}$

or, $\ln 2 = t_H / (R_A + R_B) C$

or, $t_H = \ln 2\ (R_A + R_B) C$ ..... (1)

For low output period:

$2/3\ Vcc = 1/3\ Vcc\ e^{t_L/R_B C}$

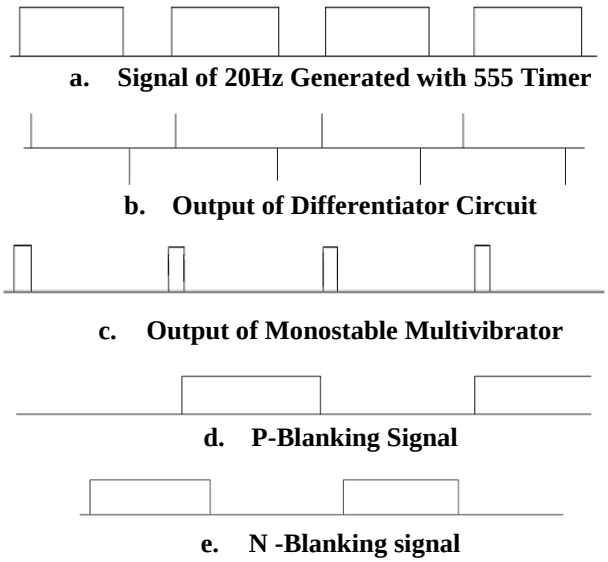
or, $\ln 2 = t_L / R_B C$

or, $t_L = \ln 2\ R_B C$ ..... (2)

Where, $t_L$ = time duration of the low level output

$t_H$ = time duration of the high level output

So the signal P (or N) can be generated by using the 555 timer. Another signal N (or P) is shifted $180^0$ from the previous signal which can't be produced by the 555 timer because in case of astable operation both N and P signals start and terminate at the same instant. Thus our condition of time delay between the signals is not fulfilled. To fulfill this, there should be a time delay in the charging or discharging of the capacitor. By generating a signal whose frequency is double than that of the P signal and then this signal is passed through the differentiation circuit to produce spikes. For generation of the delayed (N or P) signal, a monostable multivibrator is used which is triggered by these spikes. The time period of the monostable multivibrator is set to 6 msec by choosing R = 27kΩ and C = 0.22μF. This signal is passed through NOT gate along with the signal generated before. The P and N blanking signals are shown in figure 12 [10], [11].



**a. Signal of 20Hz Generated with 555 Timer**

**b. Output of Differentiator Circuit**

**c. Output of Monostable Multivibrator**

**d. P-Blanking Signal**

**e. N -Blanking signal**

**Fig. 12 P and N Blanking Signals**



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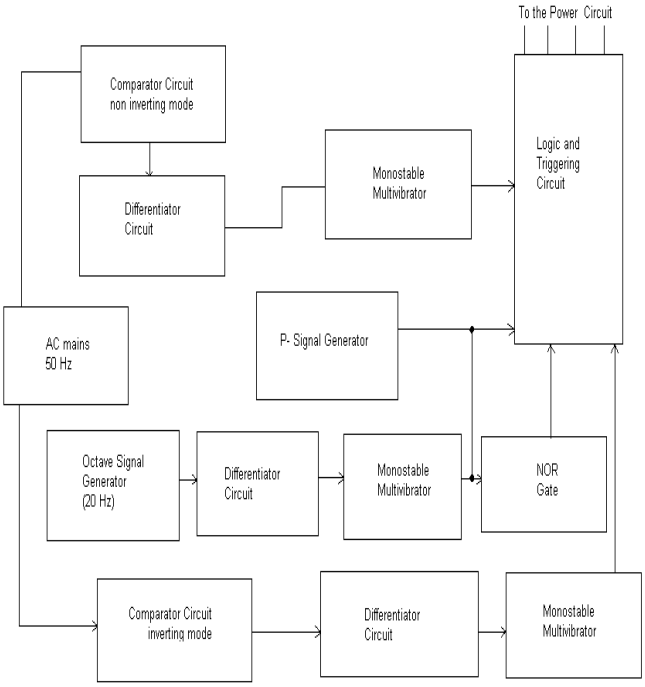


**Fig. 13 Detailed Block Diagram of the Control Circuit**

So, the time delay between P and N signals can be achieved by using the NOT gate. For synchronization between the blanking signals P and N it is required to set the charging of the capacitors of both 555 timers at the same instant. This can be achieved by using two push buttons which are normally open and they are connected across the leads of the capacitors. By pressing them before the supply is on, the capacitors will discharge instantaneously and will charge almost at same instant when the supply is on. A little delay between the charging of capacitors doesn't alter the result [1].

For designing the logic and triggering circuit it is considered that the triggering pulses $i_{G1}$, $i_{G2}$, $i_{G3}$ and $i_{G4}$ are available to the gates of the thyristors only if the respective blanking pulse (either P or N) is present. This is accomplished by using AND gate. In this circuit design three logic gates namely NOT, NOR and AND gates are used [5]. The logic gates are designed for two state operations (saturation and cutoff) of their internal transistors and the output voltage has only two levels either low or high. The block diagram of the control circuit is shown in figure 13.

### *C. Filter Section*

The filter is used to get signal of particular frequency by rejecting other frequencies. The butterworth filter has flat frequency approximation because the pass band attenuation is zero and decreases gradually at the edge of the pass band. Above the edge frequency, the response rolls off at a rate of approximately 20n dB per decade, where n is the order of the filter [9]. The figure 14 shows the frequency response of a butterworth filter. As the frequency increases the response curve decreases slowly. The major advantage of a butterworth filter is the flatness of the pass band response and the major disadvantage is the relatively slow role-off rate compared with the other approximations.

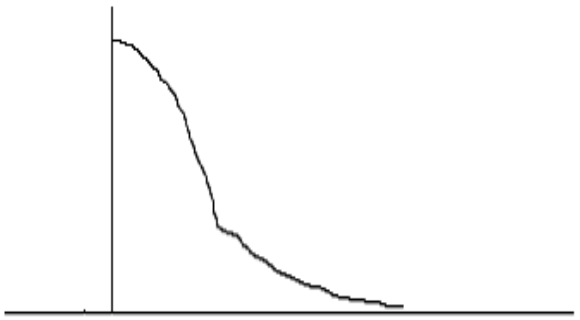

**Fig. 14 General Response of Amplitude Butterworth Filters**

Let fc and n represent the cut off frequency and order of approximation respectively for a butterworth low pass filter. The variation of the amplitude with respect to frequency in the frequency response characteristics curve is given by the following function,

$$M(w) = \frac{1}{\sqrt{1 + (f/fc)^{2n}}} \qquad \text{.....1}$$

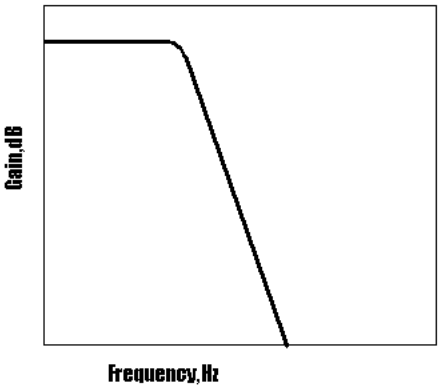


**Fig.15 Frequency Response of Butterworth Low-Pass Filter**

The frequency response of butterworth low pass filter is shown in figure 15. The maximum value of M (w) occurs at f = 0 which is unity and the filter is said to have a flat loss. Conversely, some active filters have a maximum value which is greater than unity. Let $M_{dB}(w)$ represents the decibel form of the response relative to the maximum level which can be expressed as,

$$M_{dB}(w) = 20 \log_{10} \frac{1}{\sqrt{1 + (f/fc)^{2n}}}$$

or, $M_{dB}(w) = -10 \log_{10} [1+ (f/fc)^{2n}]$

## III. DESIGN AND CALCULATION

### *A. Calculation for P and N Blanking Signals*

The ON duration of P and N signals is calculated as 49.6 msec and the OFF duration as 50.4 msec. The blanking pulses P and Q are generated by using 555 timer. The calculation for P and N blanking signals are given below,



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Off Time Calculation

$t_L = \ln 2\ R_B C$

If the capacitor is 47µF then $R_B$ can be calculated as,

$49.6 \times 10^{-3} = \ln 2 \times R_B \times 47 \times 10^{-6}$

So, $R_B = 1.5225\ K\Omega$

On Time Calculation

$t_H = \ln 2 (R_A + R_B) C$

or, $50.4 \times 10^{-3} = \ln 2\ (R_A + 1.5225 \times 10^3) \times 47 \times 10^{-6}$

so, $R_A = 24.55\ \Omega$

The blanking signal P can be generated by generating a signal with these components i.e. $R_A = 24.55\ \Omega$, $R_B = 1.5225$ k Ω and C = 47 uF and then by inverting that signal. The blanking signal N is generated in a different manner. First a signal of 20Hz is produced by using the 555 timer. Choose the capacitor C as 47 uF and $R_B$ as 500 Ω.

$t_L = \ln 2\ R_B\ C = \ln 2\ X\ 500X\ 47X10^{-6} = 16.228$ msec

So, the on time period will be (50-16.28) i.e. 33.71 msec.

$t_H = \ln 2\ (R_A + R_B) C$

or, $33.71 \times 10^{-3} = \ln 2\ (R_A + 500) \times 47 \times 10^{-6}$

so, $R_A = 534.75\ \Omega$

Therefore with the circuit parameters of $R_A$ = 534.75 Ω, $R_B$ = 500 Ω and C = 47uF, generate a signal of 20Hz with 555 timer in stable mode. This signal is passed through a differentiator circuit. The parameters of the differentiator circuit are R=10k Ω and C= 0.01uF. The RC time constant is 100usec. This signal is passed to trigger a monostable multivibrator with circuit parameters of R= 27k Ω, C= 0.22uF, $R_F$ = 10k Ω, $R_C$ =10k and transistors ($Q_1$, $Q_2$) of 2n2219A with $h_{FE}$ = 200. This signal and P blanking signal are then passed through a NOR gate in order to obtain the N blanking signal.

### *B. Calculations for Synchronizing Signals*

The first step in generating the synchronizing signal is the use of comparator circuit using the operational amplifier (741). The analog signal is taken from the ac mains. Since the operational amplifier uses a supply of 15 volts, the input must not exceed Vsat i.e. 13 volts. For this the rms value of the secondary output of the transformer needs to remain at 9 V (12.72 V p-p). Two comparators are used in both inverting and non inverting mode and the outputs of them are fed to the differentiator circuit. The parameters of the differentiator circuits are R= 10kΩ, C= 0.01µF and the RC time constant is 100usec. The differentiated signals of the differentiators are fed into the monostable multivibrator and the parameters of the monostable multivibrator are R= 10 kΩ, C= 0.22 µF, $R_C$= 1 kΩ and $R_f$ =10 kΩ. This generates train of pulses with time period of 220usec in both inverted and non-inverted mode.

### *C. Filtering the Cycloconverter Output*

The output wave of cycloconverter is of square shape with maximum amplitude of 12.72 volts. The butterworth filter can be used for filtering the output. The output wave comprises of fundamental frequency of 10 Hz and harmonics. The calculation for filter selection is given below.

The 3 dB cut off frequency is given by,

fc = 1/(2x3.14159x RC)

or, 10 = 1/(2x 3.14159 x RC)

or, RC = 1/(20x 3.14159)

Now choosing C = 100µF

so, $R \times 100 \times 10^{-6} = 1/(20 \times 3.14159)$

Therefore, R= 1.57 kΩ

So, the parameters are R = 1.57 kΩ, C = 100 µF

The sinusoidal output frequency can be obtained by passing the output through a passive low pass filter. The parameters of the low pass filter is R=1.57 kΩ, C = 100µF. The figure 16 shows the filtered output whereas the complete filter circuit is shown in figure 17.

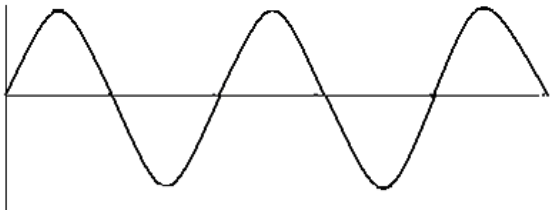

**Fig. 16 The Filtered Output of 10Hz Signal**

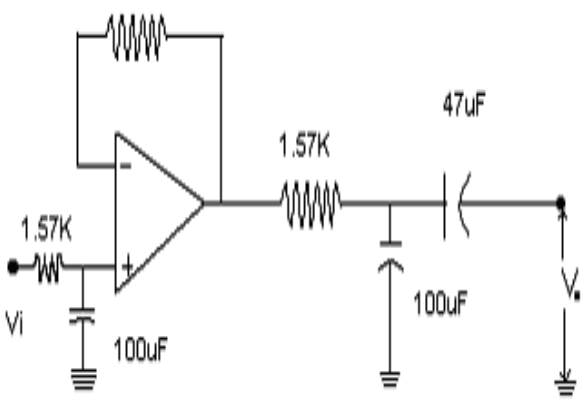


**Fig. 17 Complete Filter Circuit**

### *D. Power Calculation*

This circuit is designed for resistive load of unity power factor. The power delivery of a transformer entirely depends upon the nature of the load. So,

$VI \cos\Phi = 5000$

$VI \times 1 = 5000$

$VI = 5000$

Choosing V = 120 V and I = 41.66 A

A centered tapped transformer of secondary rating of 120V and 50A is considered for circuit design. Due to unavailability of such a large rating transformer, a cyclo cycloconverter circuit is designed with lesser power output for demonstrational purpose. A transformer of secondary rating of 9 V and 800mA is considered for designing the cycloconverter which delivers a power of about 7 W. The detailed circuit diagram of cycloconverter is shown in figure 17.



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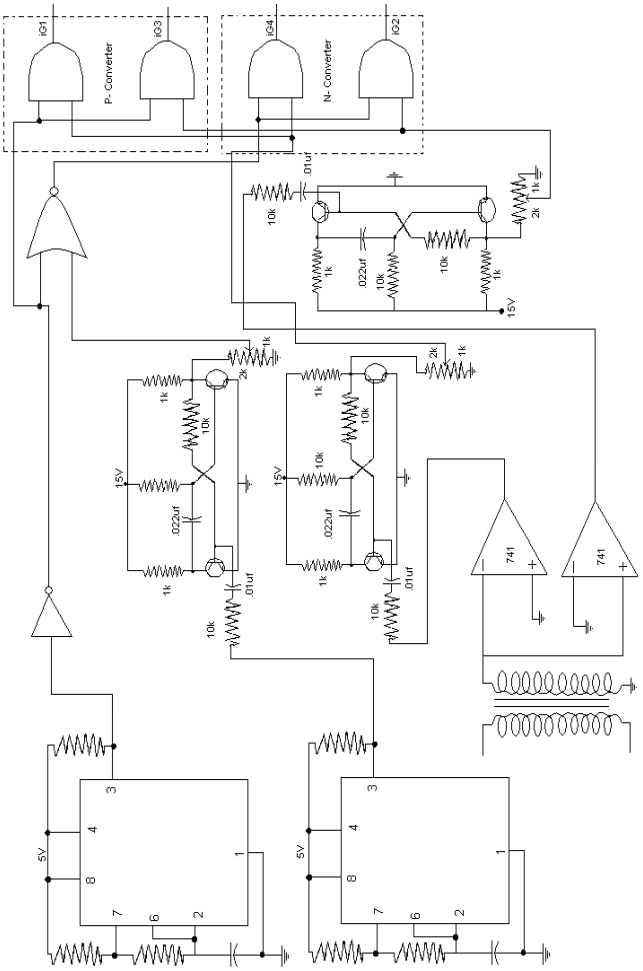


**Fig. 18 The Detailed Circuit Diagram of Cycloconverter**

## IV. CONCLUSION

In manufacturing and process industries, the variable frequency is required for driving various electrical machineries. The cycloconverter or variable frequency generator plays a significant role in driving those electrical machineries. The study mainly focuses on the design and construction of the single phase cycloconverter. The commercially designed single phase cycloconverter circuit may use different design pattern than this one. This single phase cycloconverter circuit can be extended further for three phase application. In case of the three phase cycloconverter, each of the positive and negative converter group operates for half the period of the output frequency. In this study, the proposed design of single phase cycloconverter delivers a power of 7 W.

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