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A Comparative Study of Different Low Power Techniques for SRAM

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Abstract: ***There is three type of low power technique discussed here for Static random access memory. One is Quiet Bit line architecture in which the voltage of bit line stay as low as possible. To prevent the excessive full-swing charging on the bitline one-side driving scheme for write operation is used and for read precharge free-pulling scheme is used to keep all bit lines at low voltages at all times. Second is Body bias technique which decreases the process variation on the SRAM cell and it can operate at 0.3 and write margin is not degraded. Third is half –swing Pulse-mode techniques in which Half-swing Pulse-mode gate family is used that uses reduced input signal swing without sacrificing performance and to save the power, bit lines are operated from*** V_{dd} ***/2 instead of*** V_{dd} .

Index Terms: Low power, SRAM, Body biasing, quiet bit line, Half-Swing Pulse-Mode, Low voltage.

I. INTRODUCTION

Low power, high performance SRAM's are useful in hand –held device and high performance processor. Current SRAM's routinely apply number of low power technique. At the architectural level, the key goals are localizing signals to reduce the capacitance that switches, reducing signal swings, and eliminating any dc current. Partitioned memory arrays and hierarchical word lines reduce the total capacitance that switched per access. [1] At the circuit level, designers use pulse mode circuit to improve performance and generate the pulses that are needed to satisfy the architectural demands. A pulse mode self resetting gate is faster than a normal static CMOS gate, since the forward path can be optimized for a single transition and the reset transition can be handled by the separate, self rest signal path. [2] One of the most useful techniques to reduce power is to reduce supply voltage. Multiple threshold CMOS and Variable threshold CMOS can be used to maintain good performance because as we reduce the supply voltage, threshold voltage also be lower which causes the sub threshold cell leakage current to become a significant source of power dissipation. [3] Using half –swing techniques, power needed to read data from memory and to wrtie into memory can be reduced.In this technique much of the power savings comes from operating the bit lines from vdd/2 rather than vdd.

In Quiet bitline technique there are two methods, first for read operation *precharge free pulling scheme* is used to keep all bitlines at low voltage at all times. And second for write operation, a *one-side driving scheme* is used to prevent the exessive full-swing charging on the bitlines. [6] Quiet mean that voltage of the bitlines stay as low as possible at all times. To get this condition, read and write operations need to be modified. In a *one-side driving scheme*, only strong '0' signal is forced into the cell being accessed from one side , and another side to be kept floating. *Pulling scheme* operates in four steps, bitline equalization, wordline activation, and bitline pulling, and finally sense amplification.[6]

If supply voltage is decreased , the subthreshold current also reduced exponentialy. Due to effect of V_{th} varation on sub-threshold current, working in this region causes more sensitivity to process varations. The effect of process varation is more important in circuit such as memories and flip-flop, that causing data loss on storage nodes in FFs or memories. The Process varations can be decreased by using *body biasing technique*

In this paper section II describes *Half-swing Pulse-mode* technique. In Section III *body bias* technique is discussed in detail. Section IV describes *Quiet bit line architecture* . Section V is conclusion and result discussion.

II. HALF-SWING PULSE-MODE TECHNIQUE

Without effecting performance low power SRAM can be design using half swing pulse mode gate family that uses reduced input signal swing. These gates are applicable in SRAM decoder and write circuits because it decreases the power by reducing signal swing on the high capacitance predecode lines, write bus lines, and bit lines. In [3] they used dual-V_t CMOS. To reduce the power dissipation we can keep the supply voltage low or we can reduce the supply voltage but by reducing the supply voltage transistor threshold voltage also lowered and it affect the performance.

To overcome from this problem they used multiple-threshold CMOS (MT-CMOS) and variable threshold CMOS (VT-CMOS). MT-CMOS used in decode and peripheral logic. [7][8]

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To prevent the significant leakage current high-V_t device are used, while to provide the good performance low-V_t device are used. V_t-CMOS controls the transistor threshold by varying the bias of the well and/or substrate. The power can be save by operating the bit lines from $V_{dd}/2$ rather than V_{dd}. To use $V_{dd}/2$ half-swing pulse-mode gate family can be used but it have some disadvantage because it needs level-conversion and reduced gate overdrive at receiving gates.[3]

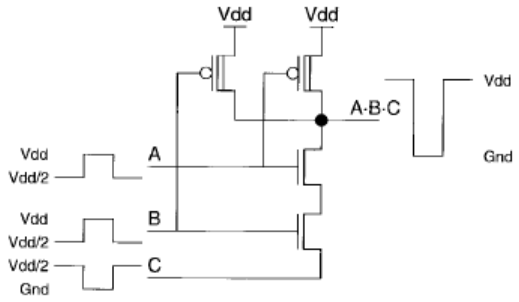

Figure 1. Half-Swing Pulse Mode AND gate [3]

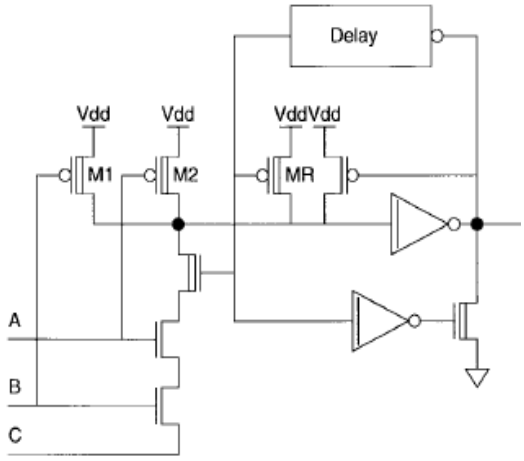

Figure 2. Self-resetting half-swing pulse mode gate [3]

This causes loss of performance. If positive half-swing and negative half swing pulse are combined with the receiver gate logic style shown in Fig.1 all of the forward transition driving transistors see a full gate overdrive, and the effect of the low swing inputs on the receiver performance is negligible. Combined with self-resetting technique this provides an opportunity to use a half swing pulsed signaling scheme which is shown in fig.2. [3]

A fixed delay after the output assertion edge, the low-V_t PMOS reset device (MR) is turned on to restore the output of the half-swing pulse-mode gate to high value. MR sees a full gate overdrive and can be sized to be relatively large since it does not strongly affect the forward transition speed. When the gate is in the rest state, waiting for input pulses to arrive, MR is off. Thus, only the extra diffusion capacitance of MR's drain affects the forward output assertion speed, but MR greatly accelerates the reset transition. The PMOS devices in the gate (M1 and M2) are only used to hold the output high after the reset pulse has been disserted. An optional low-v_t NMOS device can be added to the pull down stack to ensure that there is no fighting if the leading edge of the reset pulse arrives before the input pulse has been disserted. [3]

III. BODY BIAS TECHNIQUE

Basic CMOS SRAM cell using 6 transistors is shown in fig. 4. Storage node q and qb are shown. Assume that node qb and q stores "0" and "1" respectively. Reliability issue is important due to low supply voltage. The main leakage source in sub threshold region is sub threshold current I_{on}/I_{off} ratio in weak inversion is very low. So effect of off current to flip the data on storage node. By charging the threshold voltage, due to mismatch or process variations, the SRAM cell characteristics are changed. [5]

The body-biasing technique is used to decrease the process variation effect on the SRAM cell. Fig.3 shows body-biasing technique for SRAM cell. To control the bulk voltages of M1-M4, two inverters are added to the basic cell. Value of bulk voltage is dependent on the value stored on storage nodes. Assume that "1" and "0" are stored on q and qb nodes respectively. In that case, B2 and B1 are at "0" and "1"respectively. B2 node is connected to the bulk of M3 to "0", this helps to hold the q node in "1", so the static noise margin in read and hold is improved compared to 6T-SRAM standard cell. This improvement in SNM helps to scale supply voltage. Under 0.15V supply voltage this SRAM can work. To improve the Read SNM even more, B2 is connected to the bulk of M5 and B1 is connected to the bulk of M6. In this case the SNM is increased by 7% compared to the previous one. [3]

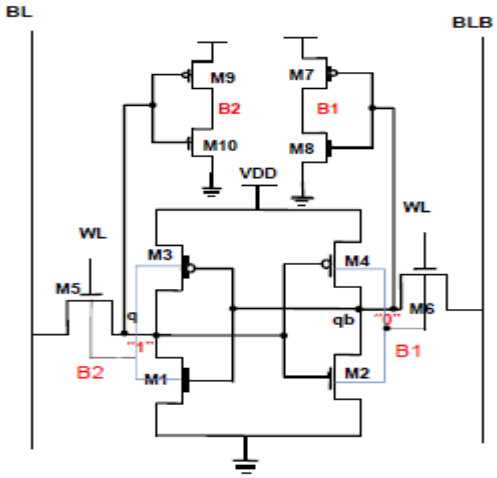

Figure 3. Proposed SRAM cell using Body biasing technique [5]

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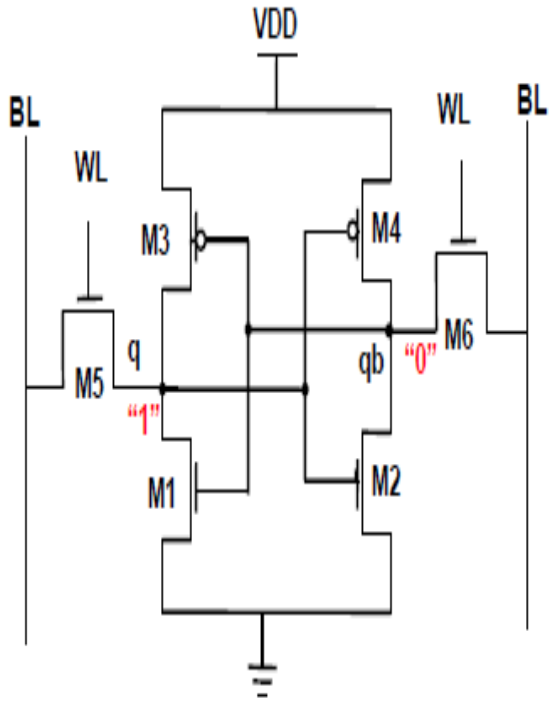

Figure 4. 6T-SRAM cell [5]

If we use body-biasing technique for pass transistor, SNM is improved around 7-10% compared to basic SRAM cell as shown in Fig.4 To see the write margin of the proposed SRAM cell, three possibilities of proposed circuit are shown. The first is the proposed SRAM cell as shown in Fig.3., second and third are connecting bulks of pass NMOS transistors to B1 and B2 and vice versa. Fig.5 shows 4 topologies that are PB1, PB2, PNB and 6T-SRAM. While PB1 and PB2 are biased for NMOS transistors, PNB has no body biasing for NMOS pass transistors While PB1 and PB2 are biased for NMOS transistors, PNB has no body biasing for NMOS pass transistors.[5]

Fig.8 shows the simulation results for write margin for different temperature for different topologies in Fig. 5. From that write margin is not degraded in PB1 but it is degraded in PB2 and PNB. The write margin is improved by 4% in PB1.For PNB; the SNM in write mode is degraded by 15%. By using PB2 circuit, the Read SNM improvement is less than PB1 and PNB. The most improvement in Read SNM is while PB1 circuit is used, but Write margin is degraded more. There are 10T SRAM cell and Dynamic Threshold-voltage MOSFET (DTMOS) cell as shown in Fig.6 and Fig.7 respectively

DTMOS SRAM cell is enables more scaling in supply voltage compared to 10T-SRAM cell to VDD=0.135V.

Fig. 9 shows the proposed circuit works in voltages enough low such as 100mV with very low failure percent.

The PB1-SRAM cell works in VDD=0.1v with less than 10% number of failures in read cycle.

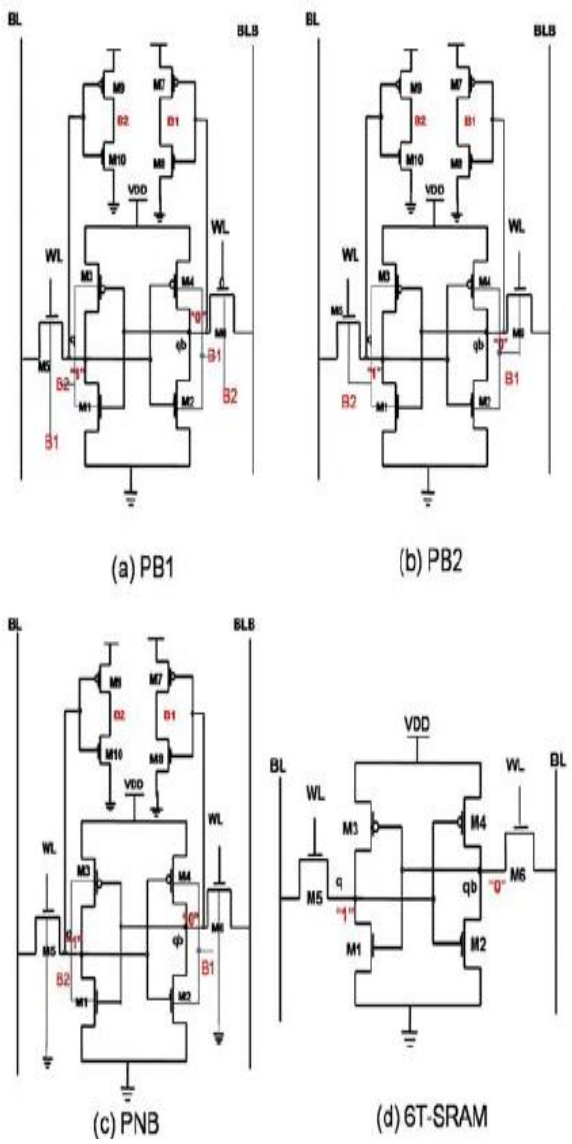

Figure 5. Different SRAM cell topologies [5]

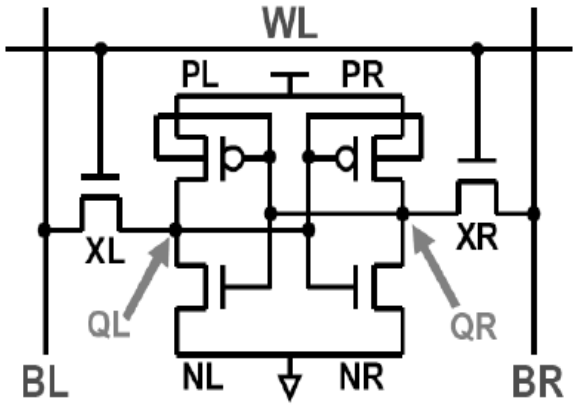

Figure 6. DTMOS SRAM cell [9]

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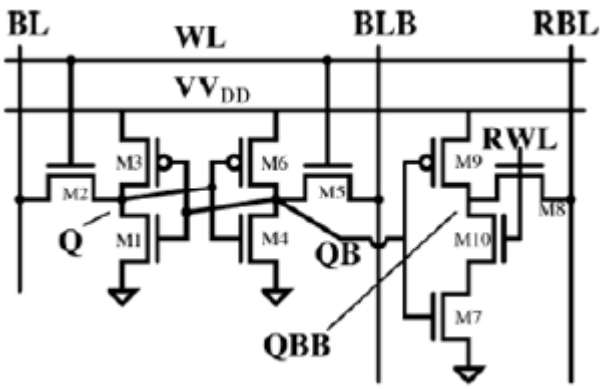

Figure 7. 10T-SRAM cell [10]

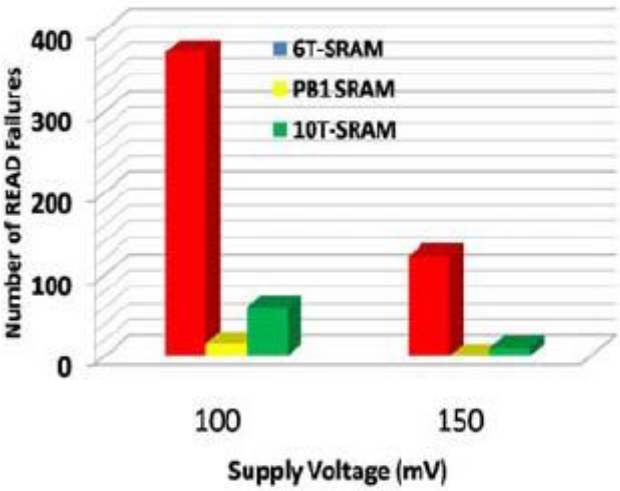

Figure 8. The number of failure in read SNM [5]

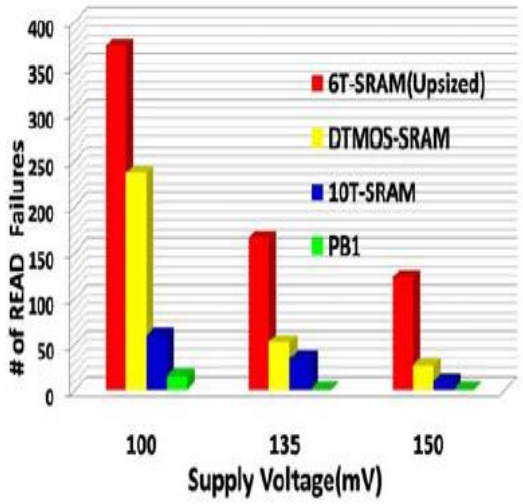

Figure 9. Read Failure in different topologies [5]

IV. QUIET-BITLINE ARCHITECTURE

By quiet mean that the voltage of the bit lines stay as low as possible at all times. The immediate reward is that all charging/discharging power associated with the bit lines can be eliminated. There are two different methods of operation for *write* and *read* operations. For write operation *one side driving scheme* is used because it is used to prevent the excessive full-swing charging on the bit lines. In this method a strong "0" signal is forced into the cell being accessed from one side, while other side is floating. For read operation *pulling scheme* is used. It operates in four steps: bit line equalization, word line activation, and bit line pulling and finally sense amplification. [4]

For a read operation, the bitline charging power can be reduced quiet significantly if the aggressive word line pulse control is used to limit the bitline swing to around 100-200mV. However, all bit lines are usually forced to have full swings during a write operation, mainly to enable a quick cell flipping.

A *one side driving* scheme in which only strong '0' signal is forced into a bitline or bitline-bar for the write operation, while leaving the other side floating. And we *remove the recharging* for both read and write operations. The combination of these two methods leads to a design with quiet bit lines. [4]

4.1 Proposed Read Operation

Like in conventional 6T-SRAM this read operation using quite bit line architecture is different in two aspects. First, there is not bitline precharging anymore. Consequently, the initial voltage of the bitline and bitline-bar before the read operation could be more diverse. Typically, the bit line pair is first equalized to a low voltage ranging from 0V to a few mV as the starting condition. Second, without the precharge transistors, the cells are the only drivers to the bitline pair after the word line is activated. Normally, we depend on the p-driver to pull up the voltage of one side of the bitline pair. The voltage of the other side could remain unchanged when the initial voltage is low, or could become lower due to the discharging by the n-driver. One major disadvantage is that there is no static power any more. In order to support such a precharge free read operation, the sense amplifier that takes the difference voltage of the bitline and bitline-bar should be able to operate over a wide of common-mode input signal range, from 0v to 500mV.[4]

4.2 Proposed Write Operation

The proposed write operation is similar to the basic write operation in terms of the bit line driving. The write buffer is still strong enough to force a value "0" into one side of the target cell. However, the cell flipping will proceed in a slightly different way. To be more specific, the cell flipping can be divided into two sub-steps:

Weak pulling: The storage node connected to the floating bit line or bit line bar only rise slowly when the word line is still activated. This is mainly because of the heavy loading of the bit line or bit line-bar and the relatively weak pulling strength of the p-driver like a static latch. [4]

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Quick latching: Right after the word line is deactivated; the target cell detaches the bit line pair and behaves like a static latch. Although the difference of Q and Q-bar at the beginning is relatively small, it will quick amplify them into complementary logic signal and thus complete a write operation. [4]

They have explained new write operation using quiet bit line architecture. Fig.10 shows column architecture and simulation waveforms of signals D, bit line, Q. they assume that the data to be written to the target cell is D=1, forcing a strong '0' signal into Q-bar through bit line-bar quickly, whiling making bit line floating. Once the stored signal Q-bar switches from '1' to '0'.its complementary signal Q will rise only slowly as in the weak pulling stage. In the waveform of signal q, this stage lasts from node A to node B. As the signal of D goes low, the signal Q rise quickly as in the quick latching stage, as indicated from node B to node C. [4]

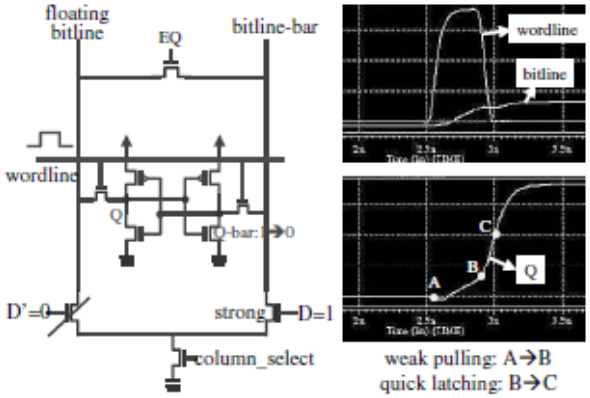

Figure 10. A write example [6]

A one-side '0' driving scheme reduces the bit line voltage swing to only 250mV- a 14% value of the power supply voltage 1.8V. It shows that power can be saved up to 86% for just avoiding the full-swing signal '1' side driving. The Moreover, the power savings are beyond that. The extra direct current flowing through the precharge transistor, access transistor, and then to the n-driver has also been eliminated. [4]

V. CONCLUSION AND RESULT DISCUSSION

Half-swing Pulse-mode technique in which half-swing pulse-mode gate is uses which is well suited for decreasing the power in SRAM peripherals circuits like decoder, and write circuit by reducing the signal swing on high-capacitance precode lines, write bus lines and bit lines.

This technique is demonstrated on a 2K×16b SRAM which is fabricated in 250nm dual V_t CMOS technology that dissipates 0.9mW operating at 1V, 100MHz, and room temperature. [3]

Quiet bit line architecture gives 84.4% power reduction compared to self-designed baseline low power-SRAM [4]

SRAM cell using body-Bias technique is simulated in a 65nm. This cell can work under 0.3V supply voltage. And PB1 cell is working under 0.1V supply voltage. If we use this technique, it increases the SRAM area. Write margin is not degraded. [5]

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