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Multiplier Design Based on Booth and Sequential Algorithm

Vaishali Sharma, R. P. Agarwal

Abstract: ***Research on cellular networks and low-power electronic devices has ramped up in recent years, thanks to the proliferation of portable and mobile systems. There are many portable applications in the present day that require low power (smaller and more efficient batteries) and more milli ampere hours than before. As a result, designing low-power devices has grown in importance as a performance criterion. Multipliers arrangement (it is an organized set of adders) and delay make up the basic construction of a infinite impulse response filter. This paper deals with analytic procedure for performance evaluation to reduce time and RAM usage throughout the computation process. The Booth and Sequential multipliers have been used to simulate, and implement in this article. Using the Sequential and Booth Algorithms, respectively. Comparative study is carried out utilising Xilinx 14.7 with the virtex 5 family, devices for bit lengths 4, 8, 16, and 32.***

Keywords: FPGA, LUTs, Memory, Booth and Sequential Algorithms.

I. INTRODUCTION

The necessity for designing and optimizing low power VLSI circuits has been driven by the demand for fast speed and little memory [1]. In signal processing, binary multiplier is digital circuit that multiplies two binary integers. Multipliers are essential parts of several highly-efficient systems, like those dealing with compression, voice enhancement, image processing, filters, & filtering. More room, more hardware, along with additional mathematical calculations are required for implementing these systems. Because it takes more time to perform a mathematical operation. Designer focuses upon adders & algorithms that will be used in multiplier architecture to achieve this. This is because delaying in propagation for carrying output & its dependence upon cascaded adders considerably impact swiftness & costing of digital apparatus [2][8]. Since there can only be two digits in binary number, multiplying any integer by another binary number always yields either zero or original value [3][5][6][7][9]. This simplifies and streamlines production of intermediate-partial products, but it slows down multiplier when it comes time to total them.

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Making partial products at the moment and summing them as they are generated, is one way to speed up this laborious job. Applications that use multiplication operations may be implemented directly utilising this method.

II. MULTIPLIER ALGORITHM

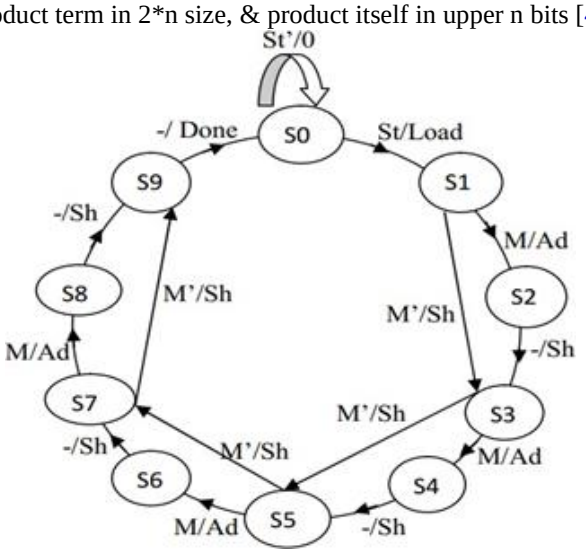
A strategy or method for multiplying two numbers is covered in an algorithm. Various algorithms are used based upon bit-length of numbers and the applications.

A. Booth Algorithm

This algorithm typically performs multiplication in two phases, generating partial products before adding them. The partial products are generated using encoding. By performing related operations upon multiplier and arranging bits of multiplicand from left to right, we may create partial product terms.

B. Sequential Algorithm

This method employs shift & add technique to optimize hardware usage. Method requires two registers, one for n-bit multiplicand and another for 2*n-bit multiplier, to perform multiplication of two 4-bit integers. Store n-size of multiplier in bottom n bits of multiplicand register, partial product term in 2*n size, & product itself in upper n bits [4].



III. SIMULATION & SYNTHESIS

Booth and Sequential algorithms have been used in the simulation and the implementation on Xilinx 14.7 with family Virtex5, device as xc5vlx50, package ff665 having speed grading of -3 for bit length 4, 8, 16, & 32, respectively.

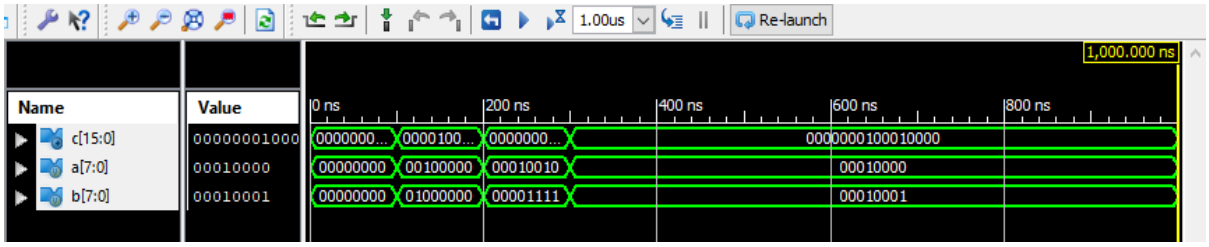


Fig-1a

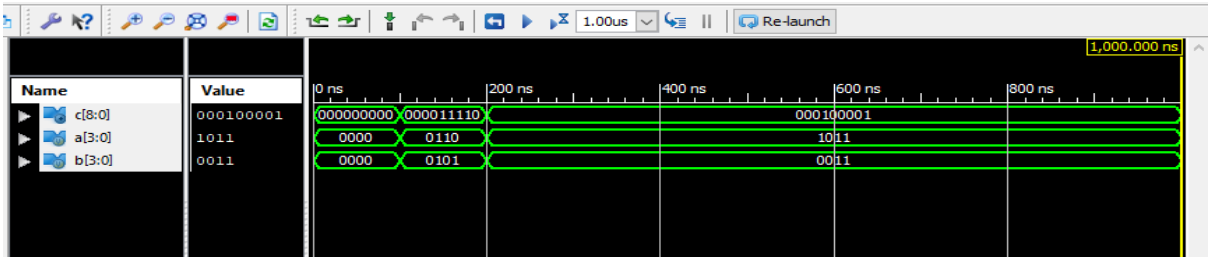


Fig-1b

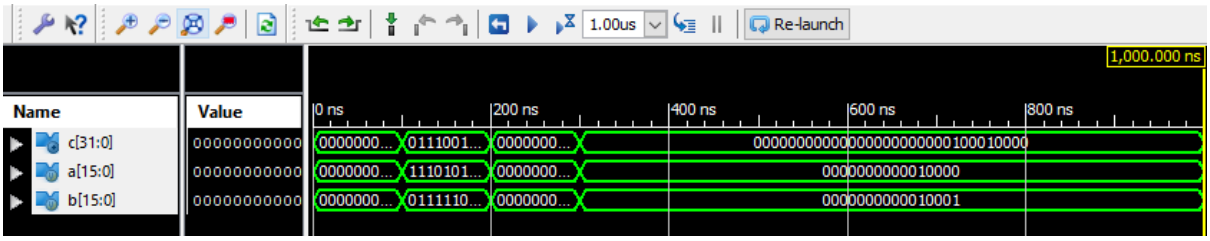


Fig-1c

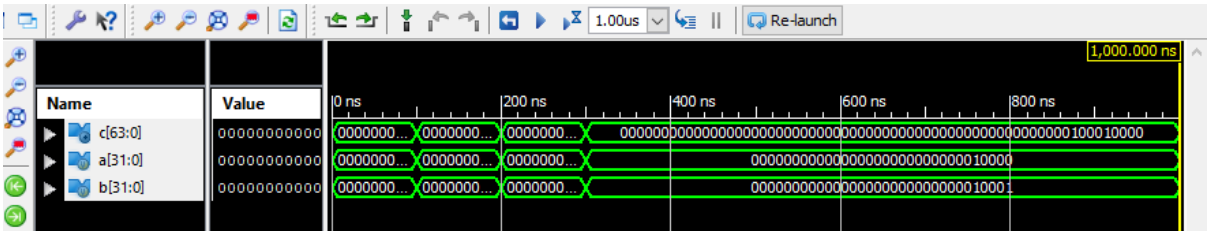


Fig-1d

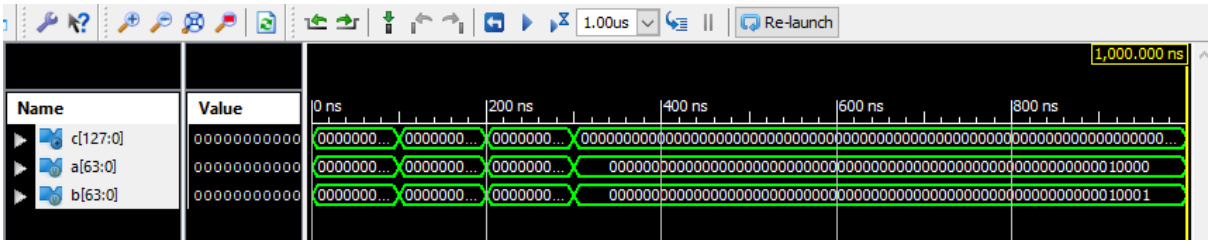


Fig-1e

Fig-1 Simulation results of 4-bit (a), 8-bit (b), 16-bit (c),32-bit (d) & 64-bit (e) of Sequential Multiplier

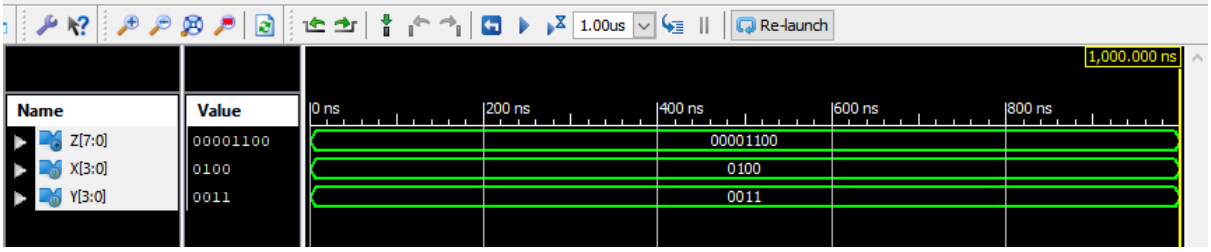


Fig-2a

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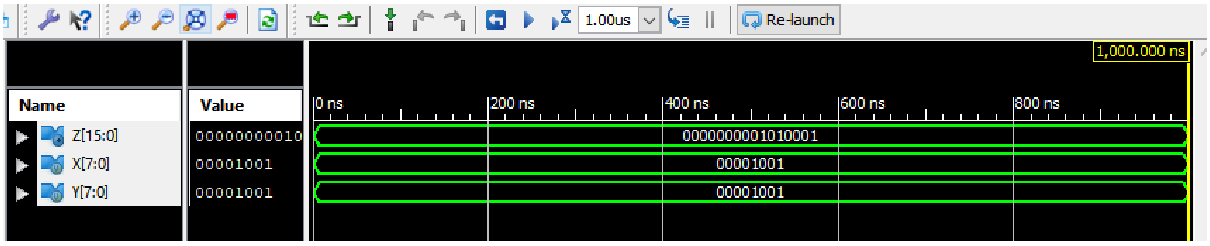

Fig-2b

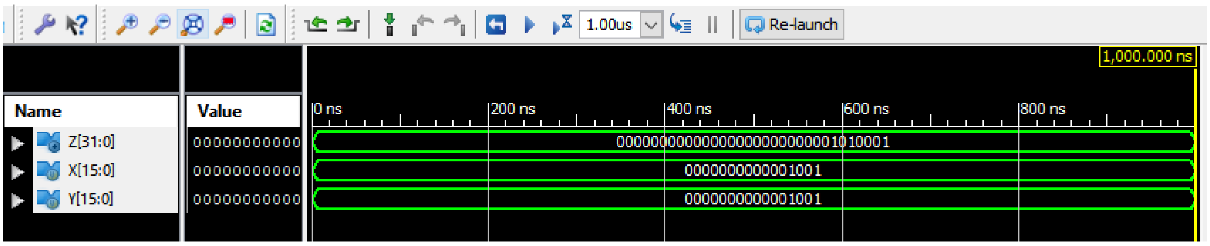

Fig-2c

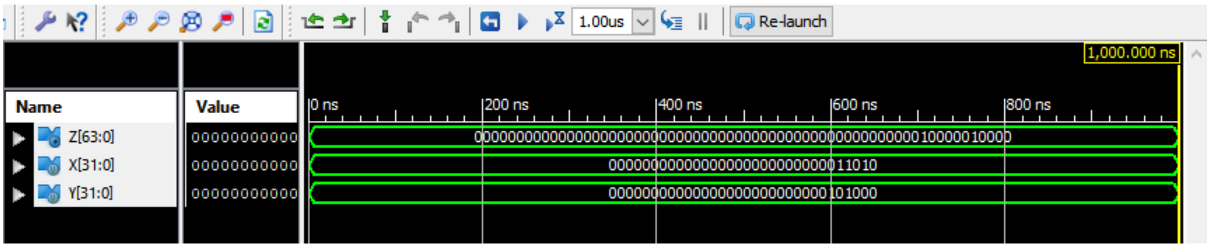

Fig-2d

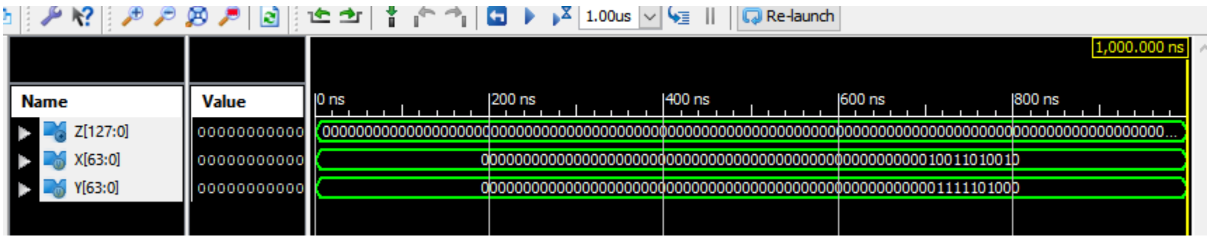

Fig-2e

Fig-2 Simulation Results of 4-bit (a), 8-bit (b), 16-bit (c),32-bit (d) & 64-bit (e) of Booth Multiplier

IV. COMPARATIVE ANALYSIS

Analysis reports (produced by simulating VHDL coding of several algorithms upon Xilinx for varying bit lengths) using MATLAB R2017 were essential in obtaining comparison findings. Table-1 displays tabular results of the simulation.

TABLE-I: Comparison b/w Booth and Sequential Algorithm for Different Bit Length of Device Virtex 5 xc5vlx50

Bit length	Type	Delay{ns}	Logic Levels	slice LUTs Count	Memory (KB)
4	Booth	5.374	5	23	4546628
	Sequential	6.803	8	20	4546704
8	Booth	15.362	30	192	4546648
	Sequential	13.763	29	94	4546712
16	Booth	25.533	63	737	4562876
	Sequential	25.657	61	382	4562844
32	Booth	45.970	128	3009	4679272
	Sequential	49.431	125	1534	4646968
64	Booth	88.869	256	12161	4887660
	Sequential	96.980	253	6142	5407860

V. CONCLUSION

The booth multiplier is the fastest in terms of speed, with a delay for 32 bits of 45.970 ns, followed by the Sequential multiplier with a delay for the same bit length of 49.431 ns, according to implementation, simulation, comparing graphs [Fig. 1(a-e),2(a-e)], and Table-I. Sequential outperforms all in terms of memory usage, using 4646968KB, compared to booth's 4679272 KB for 32-bit length. Sequential algorithm employs smaller LUTs for packing, followed by booth. Table-1 shows that as bit length increases, different algorithms' delay characteristics alter. This comparison can assist in choosing an appropriate multiplier for a specific application.

DECLARATION STATEMENT

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Ethical Approval and Consent to Participate	No, the article does not require ethical approval and consent to participate with evidence.
Availability of Data and Material/ Data Access Statement	Not relevant
Authors Contributions	All authors have equal participation in this article.

REFERENCES

1. Debarshi Dutta and Himadri Sekhar Dutta, High performance IIR flter implementation on FPGA, Journal of Electrical Systems and Information Technology (2021)1-9. http://dx.doi.org/10.1186/s43067-020-00025-4
2. N. T. Gadawe, T. A. Fathi, S. L. Qaddoori and R. W. Hamad, Synthesis and Implementation of IIR Filter using VHDL Language, 1st International Conference on Engineering and Technology,2021. http://dx.doi.org/10.1088/1757-899X/1152/1/012026
3. K. Keshav Sai Chowdary, K. Mourya and S. Ravi Teja, Design of Efficient 16-bit Vedic Multiplier. International Conference on Signal Processing and Communication. (2021)214-218. https://doi.org/10.1109/ICSPC51351.2021.9451757
4. Aniket Kumar and R.P. Agarwal, Complex Multipliers: Implementation using Efficient Algorithms for Signal Processing Application, International Journal of Recent Technology and Engineering.(2019)1235-1239. http://dx.doi.org/10.35940/ijrte.C5147.118419
5. Msughter, A., Eric, Garba, S., & Rabiu, A. B. (2023). Framing Theory Perspective of Identity and Narratives of Conflict in Nigerian Media. In Indian Journal of Mass Communication and Journalism (Vol. 1, Issue 2, pp. 1–5). https://doi.org/10.54105/ijmcj.d1039.121221
6. G, T., & K, M. (2019). Quick Response Code as a Communication Medium. In International Journal of Innovative Technology and Exploring Engineering (Vol. 8, Issue 10, pp. 4190–4192). https://doi.org/10.35940/ijitee.j1056.0881019
7. Sharma, M. R., Vardhan, K. A., Kumar, K. S., Koteswarrao, B., & S., S. K. P. (2019). Human Face Identification based on Optimal Sparse Features. In International Journal of Engineering and Advanced Technology (Vol. 9, Issue 2, pp. 690–693). https://doi.org/10.35940/ijeat.b3098.129219
8. Ahmed, A. A., & Ismail, A. (2023). To What Extent Business Excellence Dimensions Affect the Resilience and Performance of Qatari Enterprise: A Conceptual Report. In Indian Journal of Management and Language (Vol. 3, Issue 1, pp. 5–11). https://doi.org/10.54105/ijml.a2054.043123
9. NR, D., Bhagappa, & GK, S. (2021). The Smart Sailing Robot for Navigational Investigation is Used to Explore all the Details on the Zone of the Water Pura. In Indian Journal of Signal Processing (Vol. 1, Issue 4, pp. 1–5). https://doi.org/10.54105/ijsp.b1006.101321

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