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FPGA Based Efficient OFDM Based Design and Implementation for Data and Image Transmission for Healthcare

Vasanth Kumar T. R

Abstract: ***Enormous growth in the telecommunication industry demands high-speed data transmission with better quality of service (QOS). Telecommunication networks offer services with speeds ranging from 1 Mbps to several megabits per second (Mbps). However, most existing techniques aim to ensure very high-speed data for multimedia communication. Multimedia data may have suitable applications in a healthcare system. The OFDM modulation technique promises to provide multimedia services at a relatively high speed using a spectrum more efficiently compared to traditional schemes like TDMA and FDMA. The orthogonality of carriers eliminates interference among closely packed carriers, offering a comparatively efficient bandwidth. The OFDM design requires selecting proper parameters. An essential feature of OFDM is that multipaths are effectively eliminated by choosing higher cyclic prefix values, which yields significant results but causes more energy loss. This paper presents an efficient design for an OFDM transceiver using an FPGA. The design is modelled and simulated using MATLAB Simulink. Finally, the design is coded using Verilog RTL and simulated in ModelSim. Synthesis and implementation are performed using the Xilinx EDA tool. The image type of data is taken for transmission in the proposed OFDM transceiver system. The received image type data achieves a PSNR value of 29.920, and the binary input data achieves a 36.06% improvement in power utilisation and less area overhead. The paper also demonstrates improvements in area and power compared to existing authors.***

Keywords: FPGA, High Speed, OFDM, Power Optimization, Healthcare.

I. INTRODUCTION

The growth in the wireless industry justifies the necessity for multimedia transmission at much higher speeds [1]. Existing services offered by wireless companies range from voice to data. The speed of the data services ranges from a few kilobytes to Megabytes. The high-speed data is helpful for the transmission of images and data [2]. The demand for high-speed communication requires many techniques, one of which is multicarrier modulation, which is commonly used for multimedia data transmission schemes and the physical layer implementation of data transmission for WiMAX networks [3].

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*Correspondence Author(s)
Vasanth Kumar T R*, Department of Electrical Communication Engineering, AMD, Bangalore (Karnataka), India. E-mail: vasanthkumar.tr@gmail.com, ORCID ID: 0009-0008-7913-4541

The multicarrier modulation divides the data into smaller chunks of data, and these small chunks can be modulated individually using a carrier signal [4]. Multicarrier modulation has several significant features, including the avoidance of delay spread and improved spectral efficiency. The research addressed that OFDM is a popular choice for broadband networks [5]. The implementation of FFT and IFFT algorithms poses a significant challenge due to the complexity of the algorithms, which involve numerous additions and multiplications that must be performed in a short time. DSP chip and FPGA hardware are considered as the design implementation platforms for various FFT/IFFT algorithms [6]. The data processing speed needed by the VLSI technology offered by the use of FPGA, which has features like a whole environment for implementation of PSoC [7]. The FPGA is composed of millions of configurable logic blocks and other etc blocks for the RTL implementation, which makes promising answers for prototyping the ASIC using the dedicated architectures' resources for specific DSP applications [8]. The challenge for the research community is to focus on optimising VLSI designs concerning area and time. The existing methods for improving the design speed include pipelining, re-timing, etc., parallel processing etc., The paper highlights an example—FPGA-based improved OFDM transceiver design, which may be suitable for data and image transmission applications in healthcare. The performance of the system proposed in this paper is evaluated and compared with existing research work to determine the effectiveness of the proposed system in terms of area and power consumption. The paper contains the following different sections, which include the background of OFDM and a Survey of existing research. The paper also discusses the problem statement, the design and implementation of the proposed system, and finally, the results analysis.

II. BACKGROUND

The current section evolves with a discussion of the OFDM concept, which includes an overview of OFDM, the OFDM transmitter, the OFDM receiver, and issues associated with OFDM.

A. Overview of Orthogonal Frequency Division Modulation (OFDM)

The OFDM is a multicarrier modulationr transmission scheme. OFDM is a process of dividing the spectrum, resulting in multiple carriers, each of which is modulated at a lower frequency rate.

The spectrum representation of Frequency division multiplexing (FDM) is given in Figure 1. In FDM, the subcarriers are non-overlapping by which demands higher bandwidth [9].

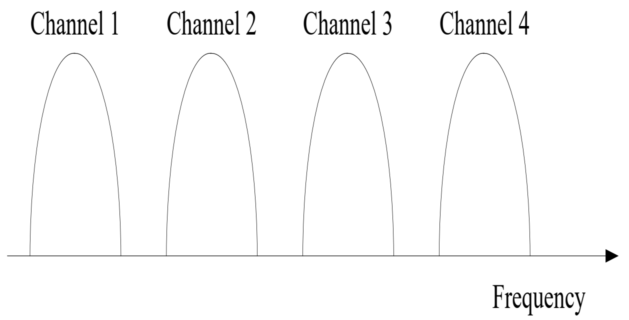

Figure 1. Spectrum of FDM

The OFDM spectrum is represented in Figure 2 with overlapping. OFDM is very similar to the FDM technique, but it is more efficient in terms of spectrum utilisation by placing the sub-channel carriers much closer. The position of subcarriers is done by selecting the frequencies which are orthogonal to each other [10].

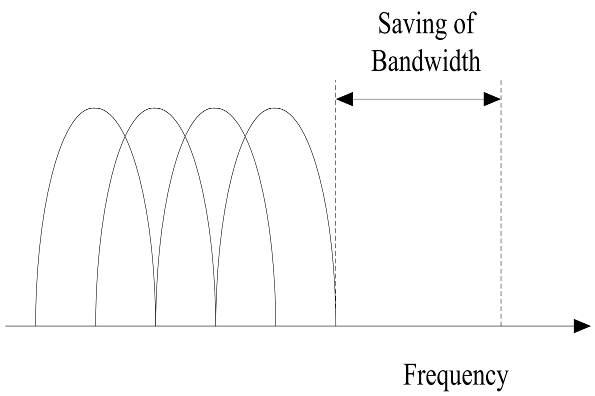

Figure 2. Spectrum Overlaps in OFDM

The orthogonality applies to both functions, whether they have real or complex values. The functions Nm(t) and Nn(t) are orthogonal over the interval p < t < q if they satisfy the condition:

$$\int_{p}^{q} N_m(t)N_m^*(t)dt = 0, \quad where \;\; n \neq m$$

The OFDM performs the splitting of the bandwidth into narrowband channels with its sub-carriers, which are made orthogonal to each other. Thus, each subcarrier spectrum exhibits a null in the centre frequency of every other subcarrier in the system and is expressed in Figure 3 below.

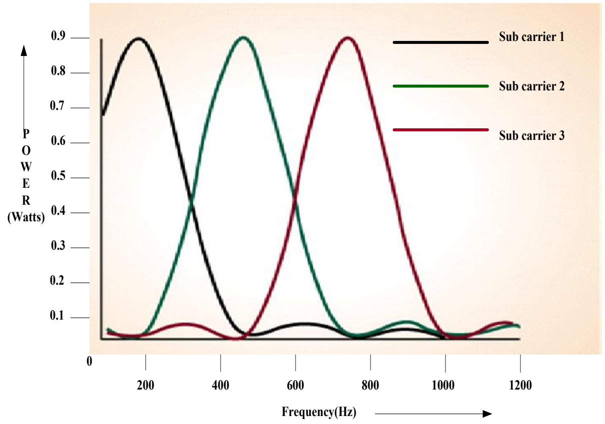

Figure 3. Orthogonality of Sub-Carriers

This leads to no interference among the subcarriers, making spacing theoretically possible. Due to this, there is no overhead associated with switching between users [11]. This helps to overcome the overhead carrier spacing issues of FDMA.

B. OFDM Transmitter and Receiver

OFDM is a multi-carrier modulation mechanism that divides a spectrum into multiple carriers, each of which is separately modulated with a low data rate signal. OFDM exhibits similar features to FDMA, where access to multiple users can be achieved by subdividing the available bandwidth into multiple channels. This can be achieved by keeping all the carriers orthogonal to one another, preventing interference [12]

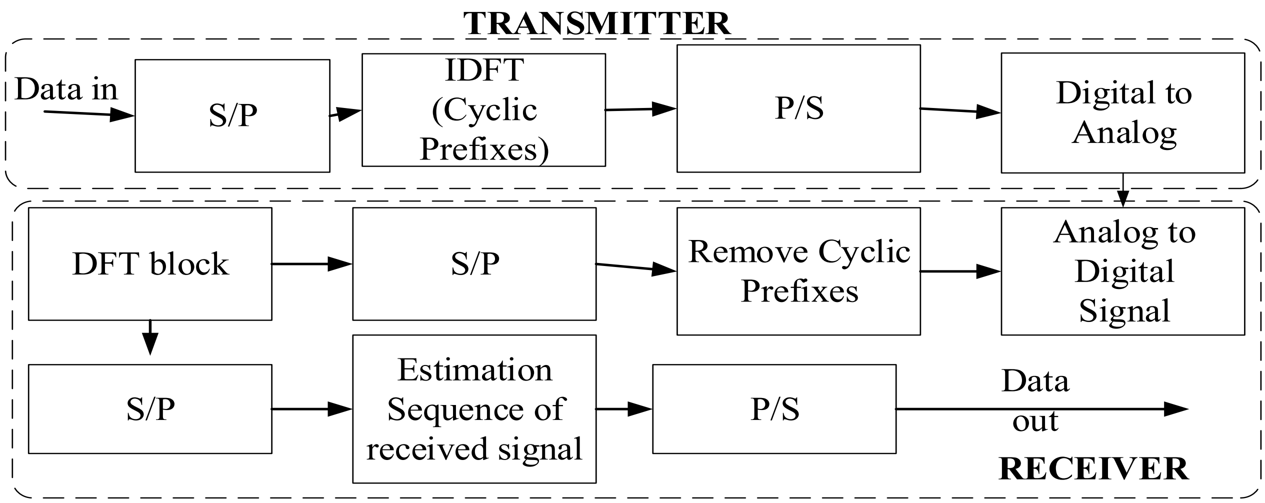

Figure 4. General OFDM Transceiver System

OFDM Significance:
The OFDM has many essential features [13, 14] than other modulation schemes and are highlighted below:

- The *bandwidth efficiency* is the main reason for high-speed communication. In wireless communication, the bandwidth can be shared by all devices expected to operate within the crowded range of carrier channels. Due to the orthogonality nature of OFDM, the total bandwidth is reduced by 50%
- ISI causes problems in high-speed *transmission*. OFDM facilitates high data rate transmission.
- The OFDM helps to spread a variety of frequency-selective fades over the symbol period. The OFDM helps randomise the *burst errors* caused by *deep fade.*

III. RELATED WORK

The work of [15] focusses on the design of IFFT algorithm for OFDM system. The design was implemented using MATLAB. The author implemented the design over an FPGA Spartan 3A, and the results were found to be effective. Similar work was done by [16] for OFDM design using the radix 2 point decimation FFT/IFFT. The design was implemented using Verilog code and simulated using Altera modelsim. The exhaustive review on OFDM for data/image transmission for various applications and research gaps is addressed, and the implementation of the FFT algorithm for OFDM transceiver is presented in Vasanth kumar and k V Prasad [17].
The system design has been improved in terms of area and speed. The outcomes suggest that the system achieves higher speed and lower area. The work introduced by Vasanth kumar [18] discussed the study on the transmitter and receiver of the OFDM system. The design is implemented using the Spartan 3A kit and coded in VHDL. The results indicated optimised and efficient outcomes.

IV. PROBLEM STATEMENT

The OFDM design requires exhaustive knowledge of selecting the critical parameters. The most crucial feature of OFDM is that, due to the nature of subcarrier level modulation with low frequency, the multipath fading is eliminated due to the increase of symbol duration, because of which a larger number of Cyclic Prefix (CP) bits are needed. This is causing more energy losses. Therefore, there is a need for a correct OFDM design concept [19, 20]. For the same concern, many researchers explored various OFDM transceiver designs by implementing the different algorithms conventionally [21]. From the survey of existing research trends in OFDM, it is observed that many of the mechanisms follow a software or C language-based approach, which may not be suitable for real-time application areas in wireless-based systems, such as WIMAX. It is found that significantly fewer proven architectures are present on hardware. These hardware architectures are designed based on OFDM and are known to have several design constraints, including area and power overhead. The existing architecture uses a Local oscillator for frequency conversion, which is an analogue-based approach. To overcome all these issues, a digital strategy is required, which necessitates RF conversion and a frequency synthesiser.

V. PROPOSED SYSTEM

To improve the analogue RF communication system, an efficient OFDM design is achieved using Verilog coding language and implemented on an FPGA platform for performance evaluation. The different blocks of the OFDM transmitter and receiver are shown in Figure 5. The figure has both transmitter and receiver blocks for the data transmission. The main components of the transmitter are the IFFT, QAM modulation and Digital up converter modules. The receiver block features FFT, QAM demodulation, and a Digital downconverter as its main modules. The input data travels through the transmitter and receiver blocks. The proposed architecture implements a pipelined 8-point 16-bit FFT. The study also implements the Upconverter and downconverter using the digital frequency synthesis (DFS) approach.

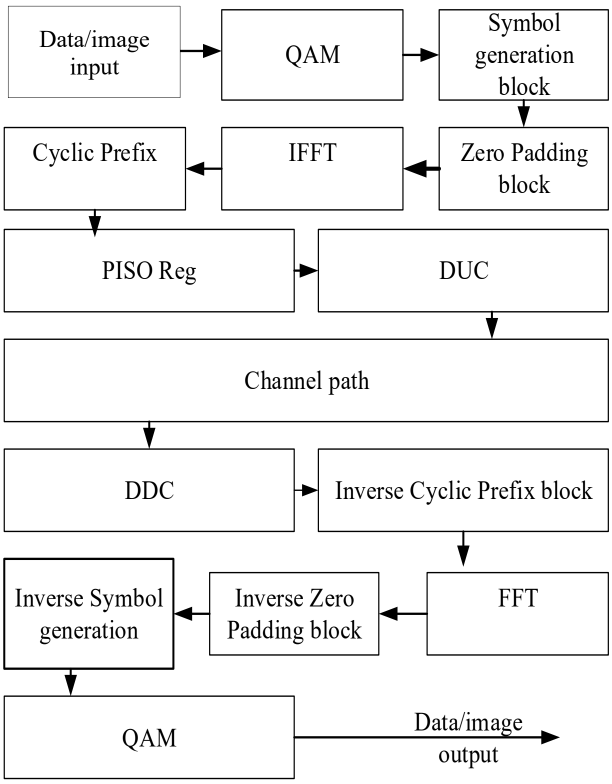

Figure 5. Architecture of Proposed System

Transmitter: This design requires a clock of 100 MHz.Different clock frequencies are achieved by dividing the global clock, which is needed by other blocks in the transmitter and receiver. The 16 QAM modulation is used for the input data. The output would be in-phase and quadrature data. The next module in the transmitter takes the 16-bit output from the modulation and produces 64 bits of symbol data. Zero padding is necessary to generate 12-bit complex data. The IFFT module performs the inverse Fourier operation on 16-bit data, and the results are stored in an 8-bit register. Therefore, there will be 128 bits of real and imaginary data outputs from the IFFT. A cyclic prefix of 8 bits to 48 bits is added to the output of the IFFT. The production of added cyclic prefix data is sent over the air using PISO. The operation of the Upconverter is to convert baseband data to several passband data.

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Receiver: The Upconverter or Downconverter block consists of a frequency synthesiser, which operates digitally, making it more efficient compared to an analogue synthesiser. This module generates sine and cosine signals based on input angle data. The sine and cosine signals are multiplexed with multipliers to give upconverter and downconverter data. The upconverter block is shown in Figure 6. The Digital frequency synthesizer architecture consists of multipliers, adders and multiplexers. Different inputs, such as xi and angle, are fed to the synthesiser architecture. Outputs of sine and cosine signals are obtained along with the register data. Later, sine and register data are multiplied to give upconverter data.

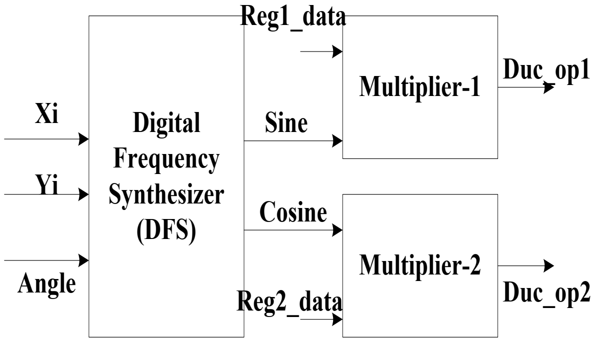

Figure 6 Upconverter Module

The specification table for the OFDM design is shown in Table 1.

Table 1. OFDM Design Specification

Channel Bandwidth BW	4 MHz
Image size	256x256
Modulation	16-QAM
FFT size	256bits
Cyclic Prefix size	48bits
Bit rate Fb	16Mhz
FFT size	256
Pilot carriers	8
Data carriers	192
Nulls	56
Maximum number of symbols	$1x10^6$
Total number of errors	500

VI. RESULTS DISCUSSION

The OFDM T design consists of a Transmitter and Receiver, as well as Upconverter and Downconverter Modules. The clock frequency used for the design is 100 MHz.The design is synthesised using the Xilinx ISE EDA tool in Verilog and simulated with Modelsim, then implemented on a Virtex 5 FPGA Board. The clock period is 10ns. The asynchronous reset is used and kept in its initial high state to reset the process. The valid input is consistently high throughout all stages. The input data is an image, and the output data is an image after the image has passed through all the receiver blocks. The following Figure.6 represents the input image at the transmitter block and the output image received with a PSNR of 29.920dB after the image data is passed through all the OFDM blocks. The input and output images are compared to obtain a PSNR of 29.920 dB and an MSE of 66.091. The execution time to complete the process is 1.31ms. The quality of the image will be satisfactory based on the above PSNR value in standard OFDM Systems. The above results are achieved when passing input data through an OFDM transceiver system developed using MATLAB Simulink. The parameters chosen for simulating the design are listed in Table 1.

Figure 7. Input and Output Image- with PSNR = 29.920 dB

The proposed OFDM system is implemented using Verilog HDL code and simulated using ModelSim. Table 2 shows the utilizatio.n of the proposed OFDM system

Table 2: OFDM System Tran.smitter Utilization

Logic Utilization	Used	Available	Utilization
Number of Slice registers	995	126800	0%
Number of Slice LUT's	5266	63400	8%
Number of fully used LUT-FF pairs	575	5686	10%
Number of Bonded	23	210	10%
Number of BUFG/BUFGCTRLS	3	32	9%
Number of DSP48E1s	16	240	6%

The proposed system also exhibits a lower power of 1.201W compared to the work [22]. The results show that the proposed system design is power-optimised, with a value of 36.08% improvement, as recorded in Table 3.

Table 3: Analysis of Power Consumption Comparison

Utilization of power	Existing [22]	Proposed	Improvements
Total Power	1.8W	1.201W	36.08%

The proposed system design's OFDM receiver utilisation is tabulated in Table 4. From Table 4, it is found that fewer resources are used, and the percentage of resource utilisation is mentioned in the table.

Table 4: OFDM System Receiver Utilization

Logic Utilization	Used	Available	Utilization
Number of Slice registers	1121	126800	0%
Number o Slice LUT's	3777	63400	5%
Number of fully used LUT-FF pairs	271	4627	5%
Number of Bonded	23	210	10%
Number of BUFG/BUFGCTRLS	4	32	12%
Number of DSP48E1s	16	240	6%

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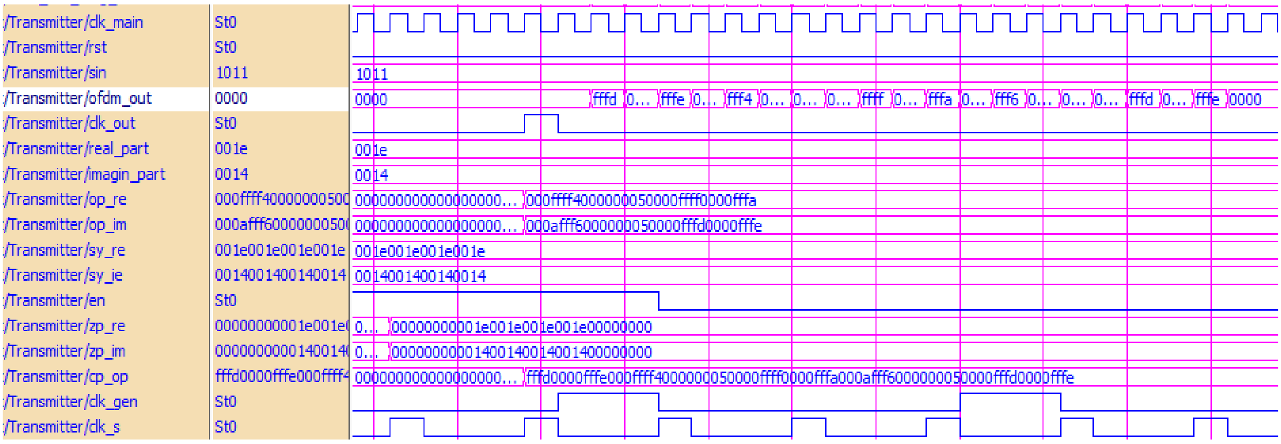

Figure 8: Proposed OFDM Transmitter Simulation Output

Figures 8 and 9 show the simulated output of the OFDM transmitter and OFDM receiver, respectively.

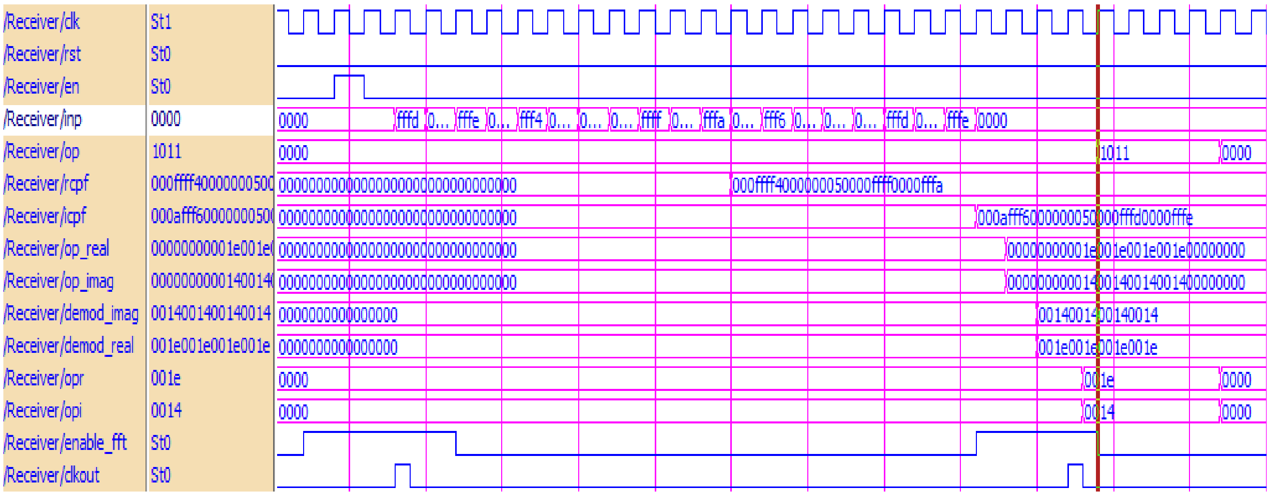

Figure 9. Proposed OFDM Receiver Simulation Output

VII. CONCLUSION

The tremendous growth in the communication industry has allowed multimedia communication to demand higher-quality service for data and image transmission at faster speeds. The challenge of optimising VLSI circuits in terms of area and power is always a research-oriented one. The existing conventional techniques for improving design speed on FPGAs involve pipelining, retiming, parallel processing, and others. Therefore, to provide high-speed data and image communication for healthcare applications, this paper presents the OFDM Transceiver design, which primarily consists of Transmitter, Receiver, Upconverter, and Downconverter Modules. The design is implemented on an FPGA platform and synthesised using the XILINX EDA tool with Verilog coding language. It is simulated using Modelsim 6.3f and Then Implemented on a Virtex 5 FPGA Board. The transmitted image achieves a PSNR value of 29.920 dB and an MSE of 66.091 with an execution time of 1.31 ms. The image quality is satisfactory based on the above PSNR value in standard OFDM systems. The paper also presents a resource utilisation summary of the OFDM transceiver system. The results obtained from the proposed system achieved total power reduction and less hardware complexity.

DECLARATION

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Conflicts of Interest/ Competing Interests	No conflicts of interest to the best of our knowledge.
Ethical Approval and Consent to Participate	No, the article does not require ethical approval or consent to participate, as it presents evidence that is not subject to interpretation.
Availability of Data and Material/ Data Access Statement	Not relevant.
Authors Contributions	I am the sole author of the article.

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AUTHOR PROFILE

Vasanth Kumar T. R. completed his Bachelor of Engineering (BE) from the University of VTU, India, and his Master's from VTU University. Completed the Ph.D. in the field of VLSI/FPGA Research areas include Wireless Communication, FPGA, 4G/5 G. He has over three decades of experience working on wireless and networking technologies. He has worked with several organisations in the past. The author is affiliated with several organisations for collaborative work.