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High Performance, Low Power Wallace Tree Multiplier

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Abstract: ***An area-efficient high Wallace tree multiplier using adders is presented in this paper. The proposed Wallace tree multiplier is designed using logic gates and adders. The design is implemented in Cadence Virtuoso using a 45-nm technology library. The proposed design offers reduced delay and higher performance than conventional multipliers using carry-save adders with majority-based gate adder logic. The design also features a reduced transistor count of 12, which is significantly lower than the traditional design. One of the fundamental building blocks of many VLSI applications is multipliers. To enhance the performance of circuits and systems, designing multipliers is essential. The key feature of a high-performance Wallace tree multiplier lies in its efficient reduction of partial product additions. By utilising a combination of carry-save and carry-propagate adders, it minimises the critical path delay and maximises the speed of multiplication. Additionally, advanced optimisation techniques such as parallel prefix adders and parallel carry-save adders can be employed to improve performance further.***

Keywords: Wallace Tree Multiplier, Carry save adder, Majority Gate Adders (MGA), low power, Cadence virtuoso tool.

I. INTRODUCTION

In conventional multipliers [Design and FPGA Implementation by Sudeep. M.C., Sharath Bimba. M.[1]], the adders used in the tree are based on ripple-carry adders, which can be slow because succeeding bits have to wait while the preceding bits are added and inefficient for multiplying significant inputs. However, the proposed method uses carry-saving adders in the Wallace Tree multiplier to improve its performance [1].

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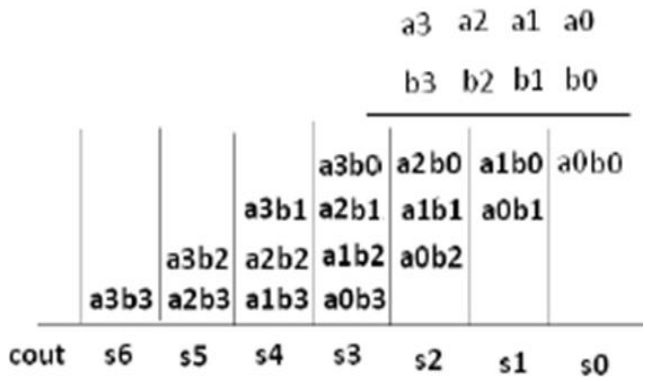

One of the main advantages of the Wallace Tree Multiplier is its speed. By breaking down the multiplication process into multiple stages, it can perform multiplication much faster than traditional methods [2]. Overall, the Wallace Tree Multiplier is a widely used architecture in modern digital circuits, especially in high-speed applications where fast multiplication is critical. A multiplier is a crucial component in high-speed digital signal processing applications. With the advancement of techniques in wireless communication and high-speed ULSI design in recent years, there is increased pressure on modern ULSI design, where the primary constraints are power, silicon area, and delay. In all the high-speed applications to very large-scale integration fields, fast speed and less area are required[2]. There are two approaches to improving the speed of multipliers: the Booth algorithm and the Wallace tree algorithm. Generally, multipliers require high latency during the partial product addition, and conventional multipliers have more stages, so the delay is more[1].

II. METHODS

In conventional multipliers, the adders used in the tree are based on ripple-carry adders, which can be slow because succeeding bits have to wait while the preceding bits are added and are inefficient for multiplying significant inputs[1].

III. WALLACE TREE MULTIPLIER:

The proposed method is the Wallace Tree Multiplier. Its architecture is used to perform fast multiplication of binary numbers. It was invented by computer scientist Andrew C. Wallace in 1964.
The architecture works by breaking down the multiplication process into multiple stages of partial products, which are then added together to produce the final result [3].

In a Wallace Tree Multiplier, the partial products are generated using simple bit-level operations such as AND and XOR gates [Wallace Tree Multiplier using Majority-Based Gate Adders by Mamudi Murasu, Sanjana Sujith, Anita Angeline, Sais Priya, and V.S. Kanchana Baskaran]. [2].
The partial products are then grouped into "partial sums" using a series of carry-save adders. These partial sums are then further added together in a binary tree structure, resulting in the final product [1].
A Wallace Tree multiplier is a high-performance digital circuit that performs the multiplication of two numbers using a tree of adders to improve its performance [1].

IV. MGA LOGIC

MGAs (carry-save adders) are based on majority logic, which is a type of logic that produces an output based on the majority of its input bits. MGAs are faster and more efficient than traditional ripple-carry adders [4]. To implement a Wallace tree multiplier using MGAs, the partial products are first generated as usual using AND gates. The outputs of these AND gates are then passed through a series of MGAs to perform the addition. The result is obtained from the final production of the MGA tree [2].
One advantage of using MGAs in a Wallace Tree multiplier is that they require fewer gates than traditional adders, which reduces the overall delay and power consumption of the circuit [4]. Additionally, MGAs can be implemented using simple logic gates, which makes them easy to design and implement. Overall, the use of MGAs in a Wallace Tree multiplier can yield a high-performance and efficient circuit suitable for a wide range of digital signal processing applications.
At this stage, the two remaining partial products are combined to form the final product.
The 4-bit Wallace tree multiplier is a relatively simple and efficient circuit for multiplying 4-bit numbers, but as the number of bits increases, the circuit becomes more complex and requires more hardware resources [2].

Architecture of a 4-bit Wallace Tree Multiplier

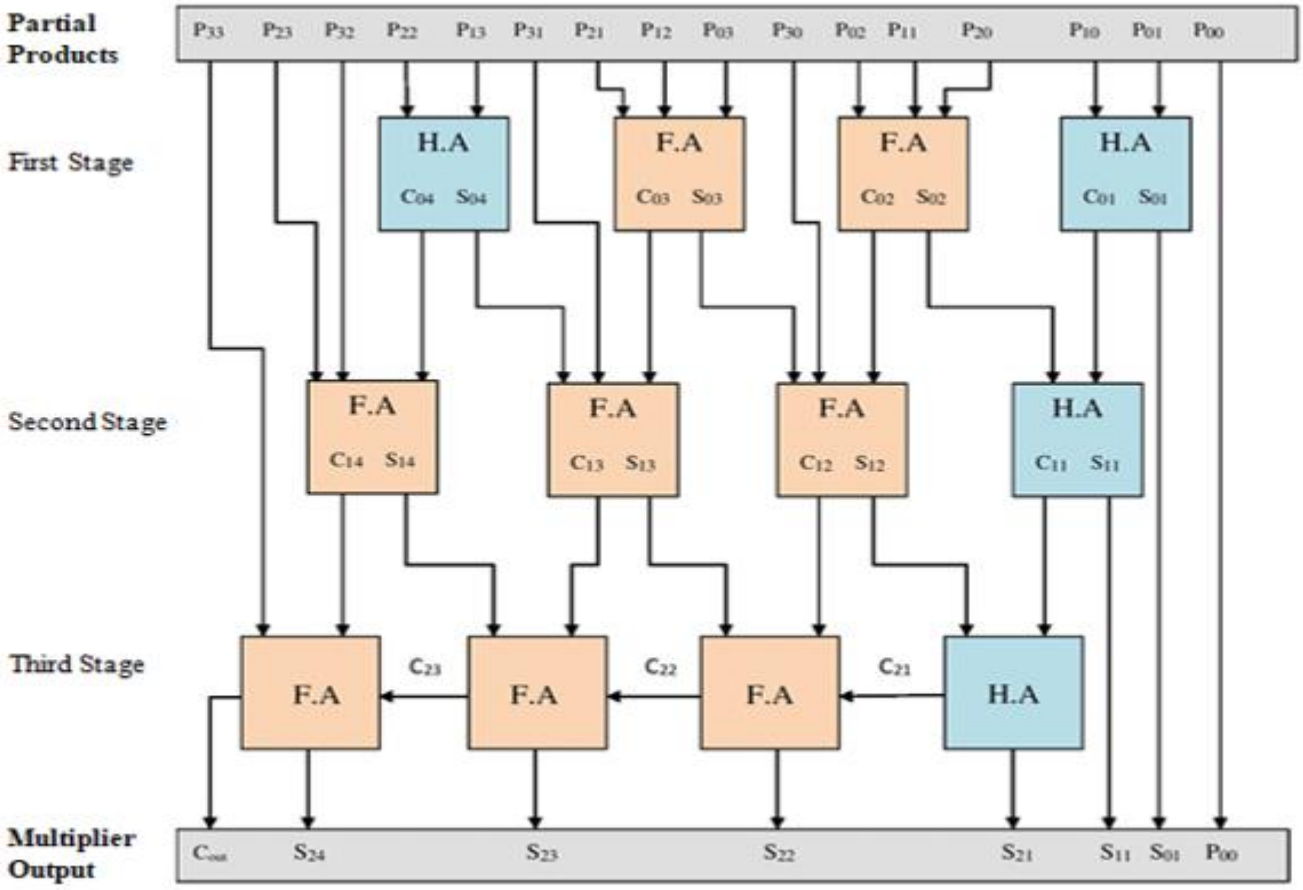

Fig no-1

V. DESIGN AND ANALYSIS:

A Wallace Tree is a high-speed multiplier architecture that reduces the number of partial products by creating groups of partial products in a way that can be added in parallel. In this example, we will discuss the design of a 2-bit Wallace Tree Multiplier [4]. The multiplication of two 2-bit numbers involves generating four partial products. Let us consider the two inputs as A = [a1=1 a0=1] and B = [b1=1 b0=1]. The Wallace Tree Multiplier for 2-bit numbers can be designed using the following steps.

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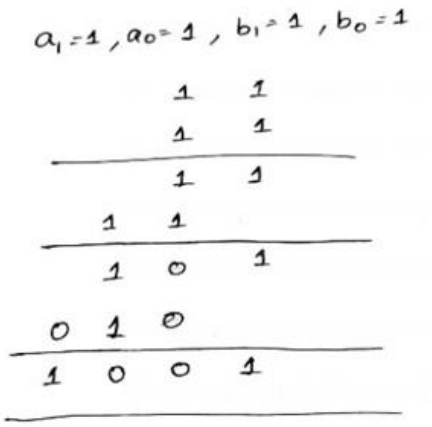

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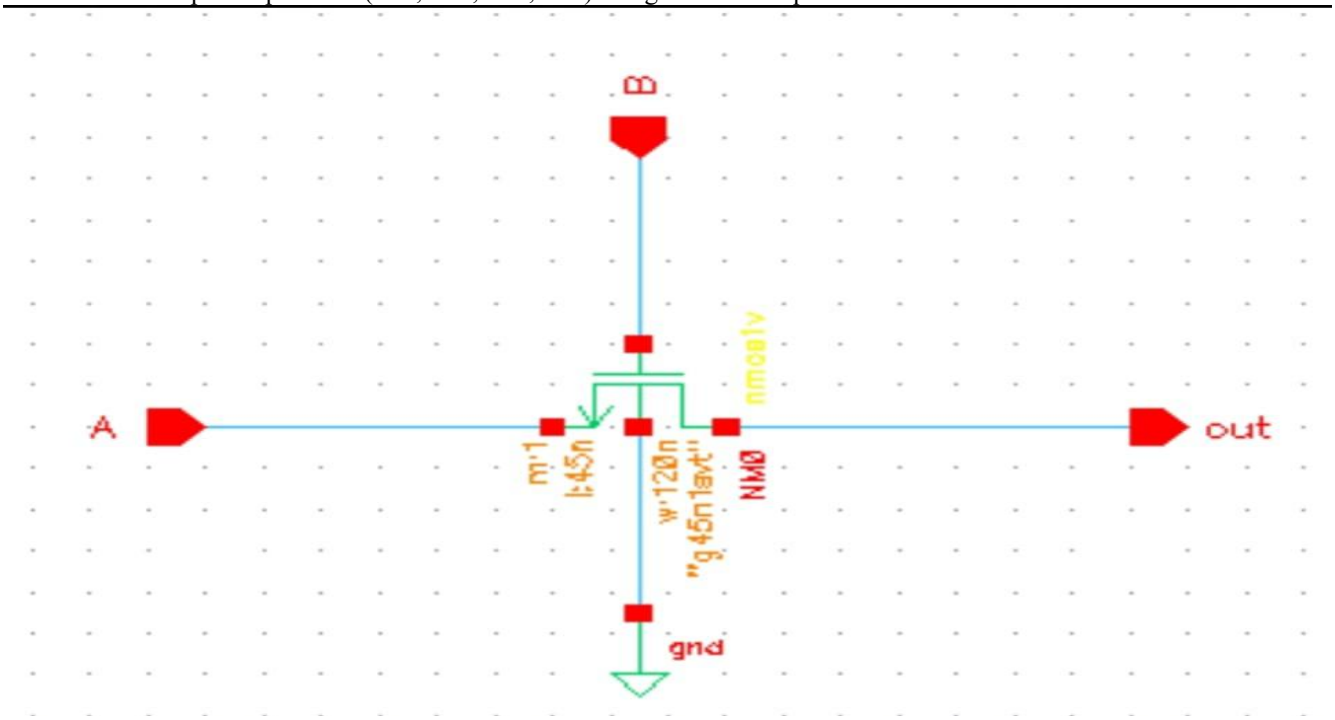
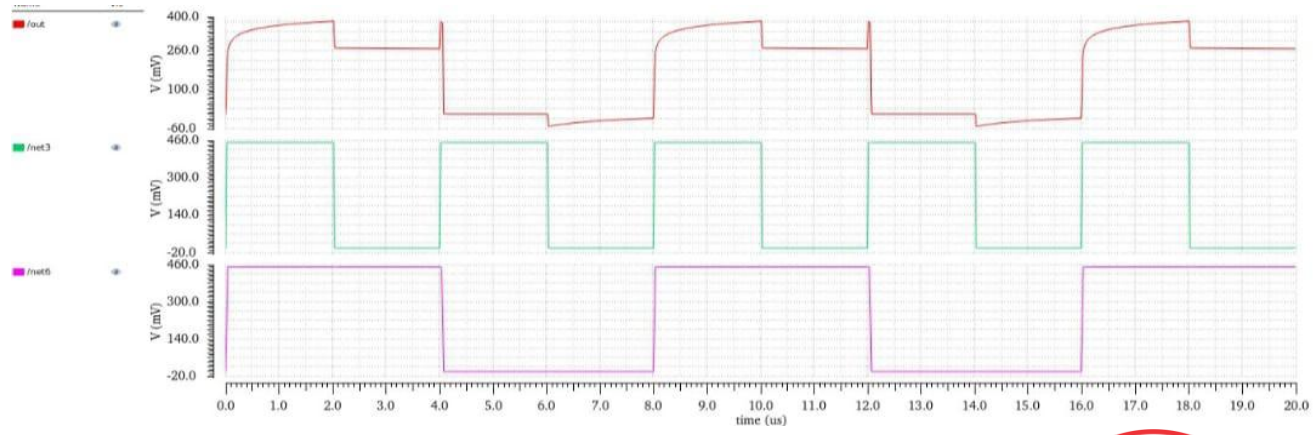
VI. IMPLEMENTATION

Step 1: Generate Partial Products
Generate the four partial products (PP0, PP1, PP2, PP3) using the above equations.



Output:



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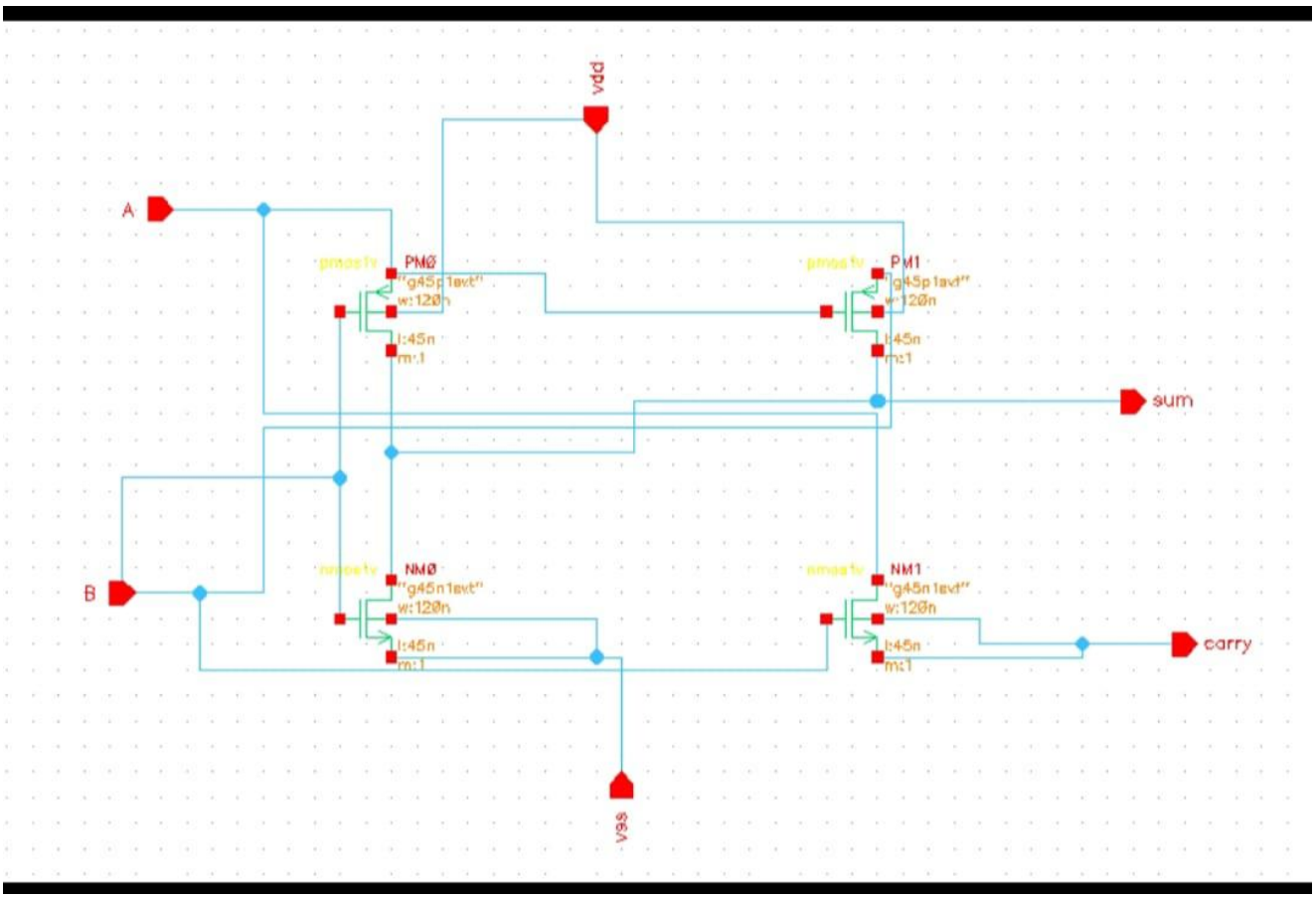
Step 2: Generate Groups
Create groups of partial products in a way that can be added in parallel. In a 2-bit Wallace Tree Multiplier, the groups are formed as follows:
Group 1: {PP0}
Group 2: {PP1, PP2}
Group 3: {PP3}
Step 3: Generate the Carry Tree
Create a carry tree to add the groups in parallel. In a 2-bit Wallace Tree Multiplier, the carry tree is formed as follows:
For this, we need to design a half adder in the Cadence tool.



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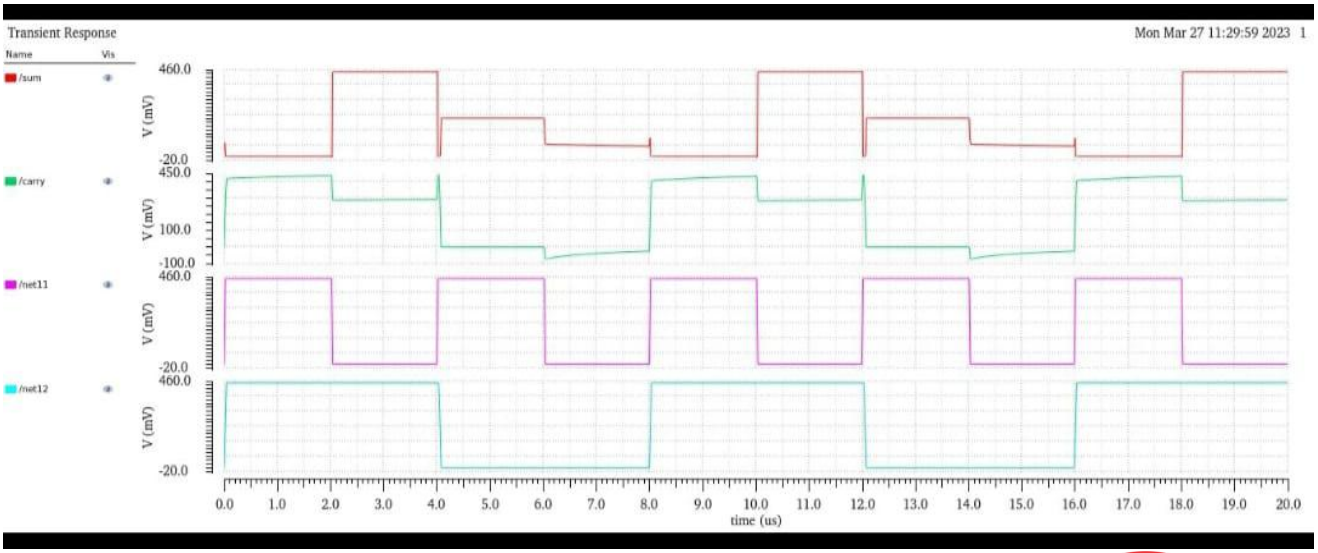

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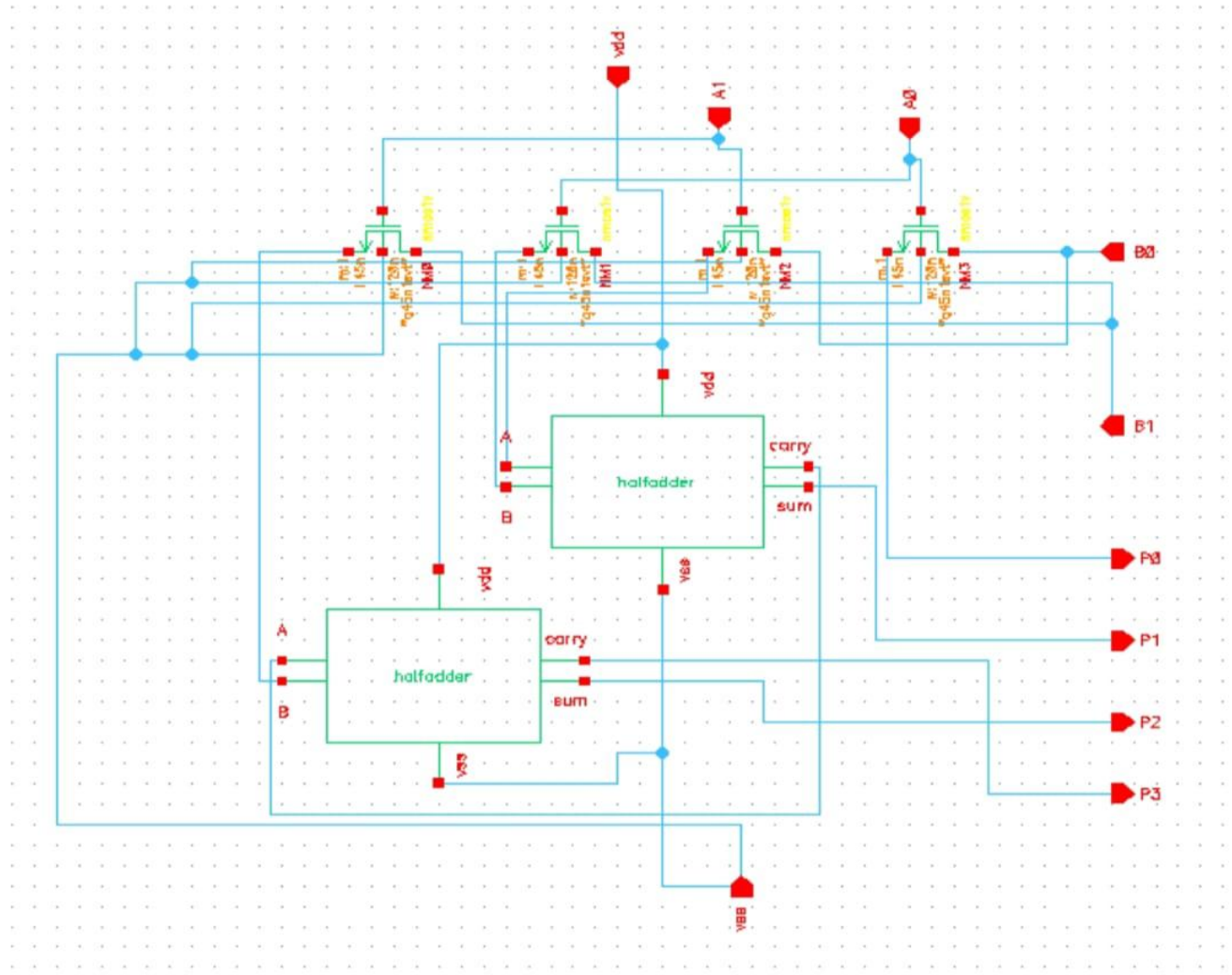
Step 4: Add the Groups

Add the groups in parallel using the carry tree. The addition of each group can be performed using a full adder. The full adder takes two inputs (the two partial products in the group) and a carry-in (generated from the previous group) and produces two outputs: a sum and a carry-out. The carry-out is passed to the next group as a carry-in. The final production of the Wallace Tree Multiplier is the sum of all the partial products.



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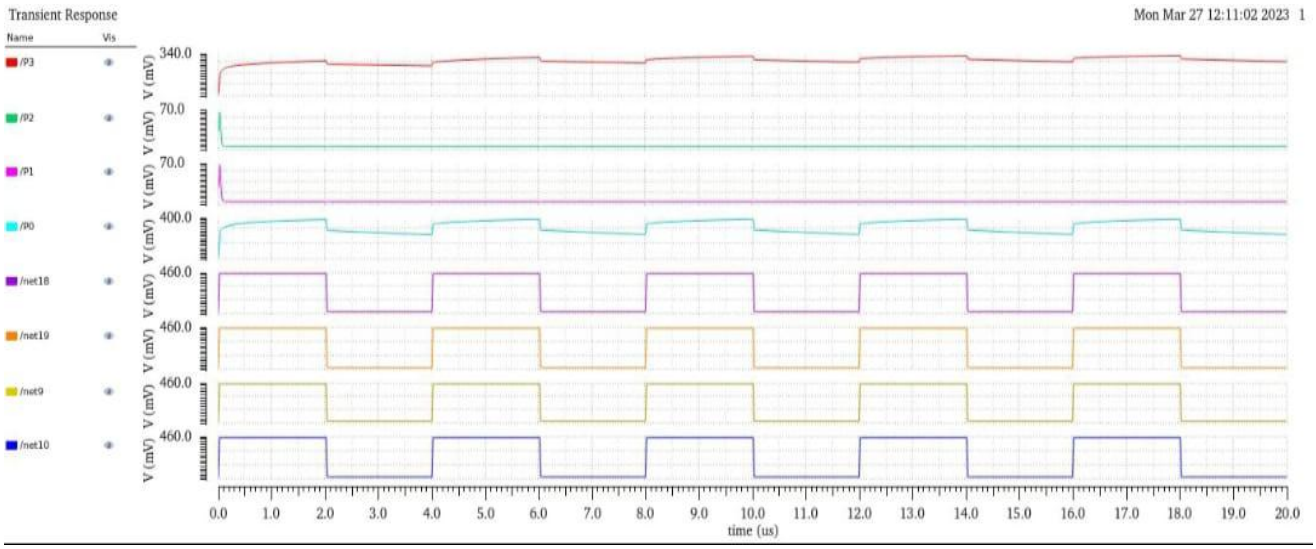

VII. CONCLUSION

It can be concluded that the Wallace Multiplier is superior in all respects, such as speed, delay, area, complexity, and power consumption. However, the array multiplier requires more power consumption and provides the optimum number of components needed, but it has a larger delay. Hence, for low power requirements and low delay requirements, the Wallace tree multiplier is suggested. This provides efficient algorithms or formulas for multiplication, which enhances the speed of devices. The average power of the proposed Wallace tree multiplier is 184.7E-6

Performance metrics	Wallace tree multiplier with 16T	Wallace tree multiplier with 12T
Power (micro watts)	200.4	184.7

DECLARATION

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Ethical Approval and Consent to Participate	No, the article does not require ethical approval and consent to participate with evidence
Avail.ability of Data and Material/ Data Access Statement	Not relevant
Authors Contributions	All authors have equal contributions to this article.

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