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Design and Implementation of High Speed Low Power Decimation Filter for Hearing AID Applications

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Abstract: ***This work is focused on designing and implementing a decimation filter specifically intended for use in hearing aid applications. The filter utilizes distributed arithmetic (DA) and is described in this brief. Our proposal involves the development of a reconfigurable finite impulse response (FIR) filter that utilises both offset binary code (OBC) and binary distributed arithmetic (DA) techniques. Additionally, we utilise canonical signed digit (CSD) representation to develop decimation filters, which include the CIC filter, half-band filter, and corrector filter. In this work, we have implemented a decimation filter using Matlab Simulink. We have utilized Xilinx Vivado 19.2 to execute the FIR filters, binary DA filters, and OBC DA-based filters. Our focus is on implementing these filters using VLSI architecture to achieve low power consumption, reduced latency, smaller area, and faster speed.***

Keywords: ***FIR filters, CIC filters, VLSI architecture, Verilog.***

I. INTRODUCTION

Due to their ability to require less hardware and process data faster, digital filters are becoming increasingly common in wireless and audio applications. While only about 5% of the world's population with hearing loss use hearing aids, designing and implementing a high-speed, low-power decimation filter using VLSI architecture can be challenging. Achieving the necessary performance characteristics requires careful consideration of several important factors, including filter architecture and digital filter design methodologies. Once these factors have been addressed, the next step is to implement the filters using VLSI technology. By balancing all of these factors, it is possible to achieve the necessary performance characteristics for a range of hearing aid applications. There are two main categories of hearing aids. They are analogue hearing aids and digital hearing aids. The input signal is converted to an electrical signal by analogue hearing aids. In contrast, digital hearing aids convert the incoming signal to binary numerical information. Because they are more adaptable and self-adjusting, digital hearing aids are generally preferred over analogue ones. Normal human hearing ranges from 20Hz to a maximum of 20KHz. The human ear often responds more reliably to auditory signals in the 1KHz to 4KHz frequency range. The block diagram of a hearing aid is displayed in Fig.1. The Preamplifier, A/D converter, digital decimation filter, and D/A converter are all included in the block diagram. The proposed architecture in this work is designed to minimise the hardware requirements, power consumption, and latency. Using CSD representation, a half-band FIR filter and a corrector FIR filter are developed and created.

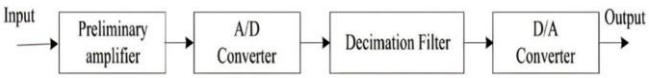

Fig.1. Block diagram of a hearing aid

II. DECIMATION FILTER

Decimation is the conversion of a signal's sample frequency to a lower sampling frequency. Downsampling is another name for it. A decimation filter [1], which is a sort of digital filter, lowers a signal's sampling rate by a factor of m, where m is an integer. Decimation filters are frequently used in hearing aid applications to reduce the signal's data rate, thereby increasing battery life and lowering the device's overall power consumption. Fig.2. shows the block diagram of a digital decimation filter. The five-stage comb filter, half-band FIR filter, and corrector FIR filter make up the bulk of the digital decimation filter (divide by 16). Comb filters have an input frequency of 1.28 MHz and an output frequency of 80 kHz. They are used as inputs for half-band FIR filters, which create an output frequency of 40 kHz, and corrector FIR filters, which produce an output frequency of 4 kHz.

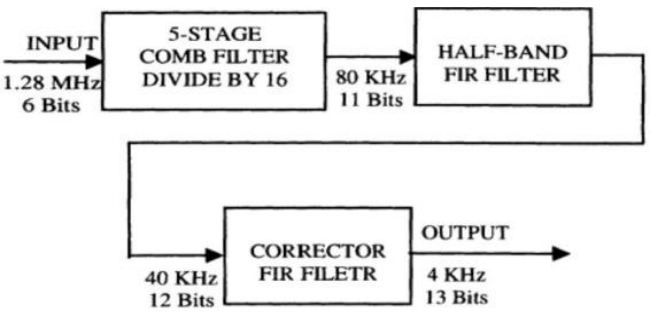

Fig. 2 (Frequency response of half-band filter)

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The initial block of a digital decimation filter is called a CIC (Cascaded Integrated Comb), and it consists of an integrator section and a comb section. The comb carries out differentiation on the signal, while the integrator carries out signal integration. Electronic equipment utilises CIC filters for various purposes, including frequency selection and extensive sampling. Unlike conventional digital filters, CIC filters do not require multipliers or coefficient storage components. Hence, operating at a fast rate of speed can be effective. Fig.3 is the block diagram of the CIC filter. The second block of the digital decimation filter is the half-band FIR filter. The half-band FIR filter receives the CIC's decreased frequency and processes it. A half-band filter is a low-pass filter that reduces the maximum bandwidth of sampled data by a factor of 2. As a result, the frequency is decreased further before being transmitted to the corrector filter. The third block in the digital decimation filter is the corrector FIR filter. Unwanted signals are eliminated using the corrector FIR filter. The corrector filter receives the lowered frequency from the half-band FIR filter and outputs it at 4 kHz. Canonical signed digit architecture was used in the construction of these half-band and corrector filters[5].

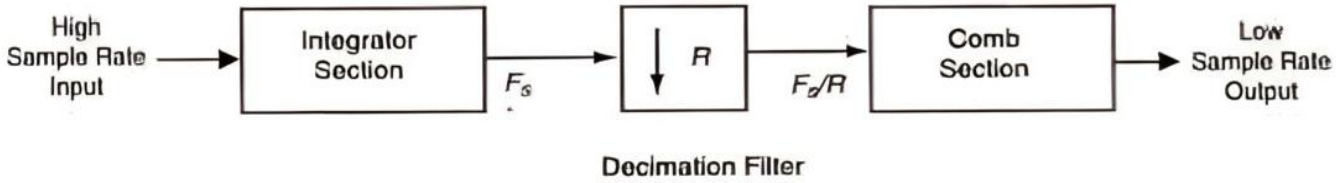

Fig.3. Block diagram of CIC filter

III. DIGITAL FIR FILTER

One of the key building blocks in Digital Signal Processing (DSP) systems is the Finite Impulse Response (FIR) digital filter. FIR filters are commonly used for a variety of signal processing applications due to their linear phase response and ability to achieve high selectivity. However, implementing FIR filters in real-time can be a challenge, as the number of Multiply-Accumulate (MAC) operations required for each filter increases linearly with the filter order. While MAC operations can consume a significant amount of resources, techniques such as pipelining and parallelisation can be employed to optimise MAC performance and reduce power consumption. Fig.4. shows the architecture of a basic FIR filter.

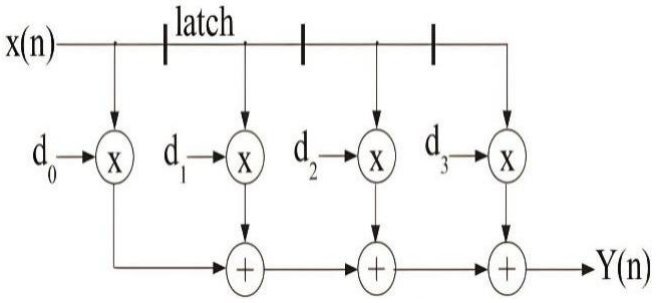

Fig.4. Basic FIR filter

A digital-to-analogue (DA) filter is a filter used to tame a digital-to-analogue converter's output waveform [2-4]. The analogue signal is cleaned up of unwanted high-frequency noise and other abnormalities. Applications that require high-quality analogue signals, such as those in audio instruments and equipment, often employ DA filters. Although the slowness of DA due to its bit-serial structure may appear to be a drawback, its ability to mechanise is a positive feature. The time needed to input K words one at a time in parallel, however, is precisely the same as the time required to input all K words serially on K simultaneous wires when the number of input words K is proportionate to the number of bits in each input word N. A sign bit timing signal, control signal S, is shown in Fig. 5. In the time of the sign bit, S is equal to 1, and 0 otherwise. One clock cycle is thought to be the length of the delay in the accumulator loop. Switch SW is in position 1 for the remainder of the clock cycle and in position 2 for the sign bit time. The completely formed result is available at the

The Accumulator's output when switch SW toggles to position 2 for one clock cycle. Shift register, LUT, adder/shifter, and accumulator units comprise the Modified Binary DA-based FIR architecture, as shown in Fig.6. The information in the ROM is the same as the information in the binary DA's ROM's upper half [6]. The adder/shifter unit's control line S can be changed to decrease the memory size of the LUT. Thus, as compared to FIR, the memory size of LUT is reduced from 2^{2K} to 2K

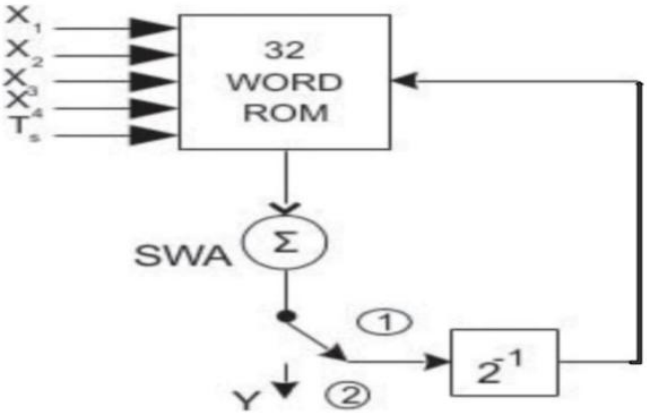

Fig.5. Binary DA

The Oversampling, Bit-stream, Closed-loop Digital-to-Analogue (OBC DA) filter is a type of DA filter that achieves high-resolution digital-to-analogue conversion through oversampling. A closed-loop feedback system [7-8] is shown in Fig. 7. This type of filter is commonly used in applications that require high-quality audio reproduction, such as high-end audio equipment and studio recording systems. Instead of using binary data, OBC DA uses signed data, or (-1, 1) (0, 1). Offset-binary code (OBC) can be utilized to shrink the size of the LUT in this case. As a result, the memory size in OBC DA is lowered from 2K to 2(K-1) [9-12].

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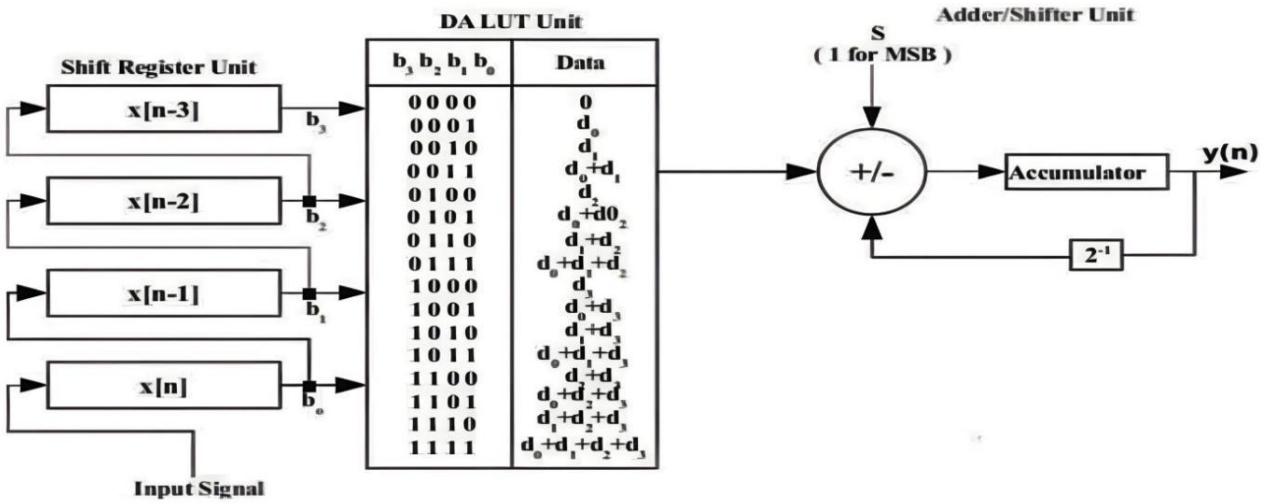

Fig.6. Modified Binary DA

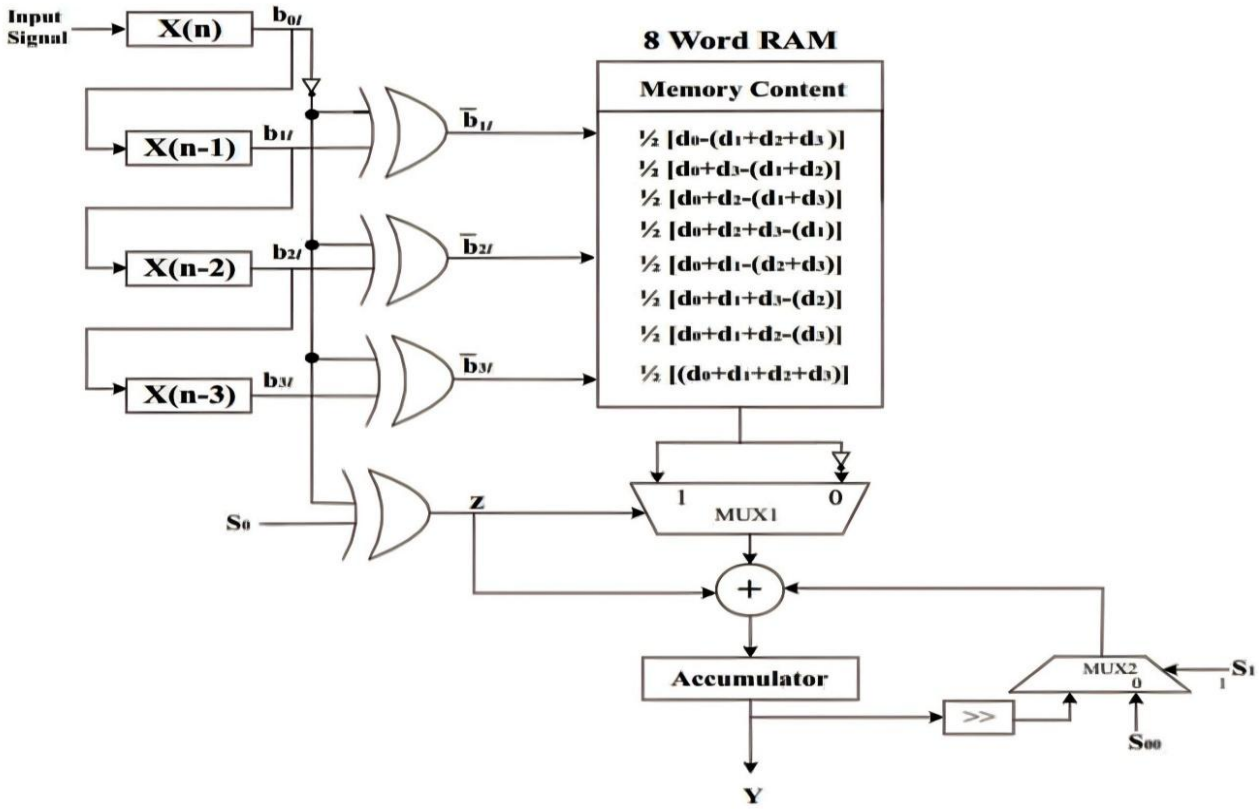

Fig.7. OBC DA

IV. RESULT AND DISCUSSION

In this work, simulations were performed on different FIR filter architectures, and a Verilog hardware description language was written for each architecture. The RTL code was then simulated on Xilinx Vivado to verify the syntax and logic functionality, and synthesis was performed to determine the area, power, and delay. The simulation results showed that the FIR filters were logically matched, and the OBC DA filter had better power efficiency compared to the DA-based filter. The simulation waveforms are shown in Figure 8a, 8b, and 8c. The synthesis report for power, area, and delay comparison is presented in Table 1. Finally, a decimation filter was designed using MATLAB Simulink. The black box window was called in the MATLAB Simulink software, and the Verilog code of our FIR filter was invoked to simulate the decimation filter for down-sampling. The simulation results from MATLAB Simulink are shown in Figures 9a,9b, and 9c. Simulation results show that OBC DA has lower power consumption compared to conventional FIR filters, and it has been successfully implemented with Verilog code and verified for a down-sampling decimation filter. Therefore, it is being used in hearing aid applications.

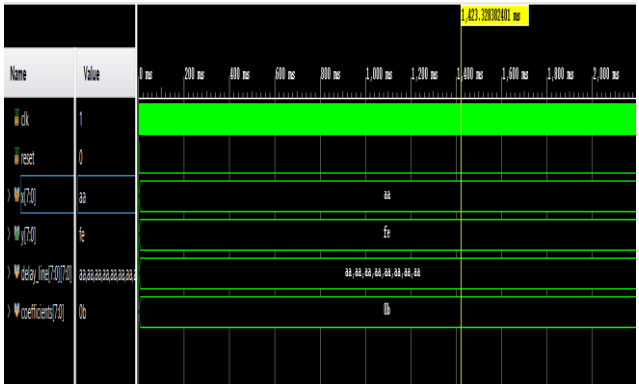

Fig8a. Simulation waveform for the FIR Filter

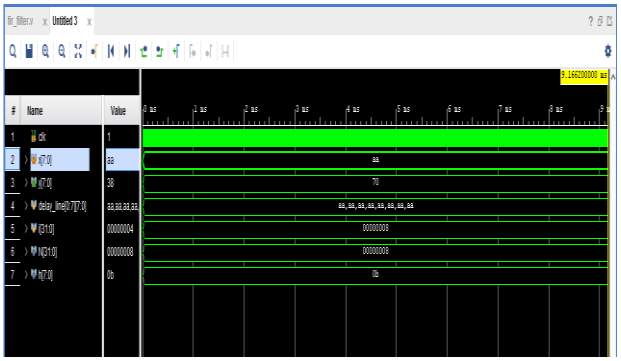

Fig8b. Simulation waveform for DA Filter

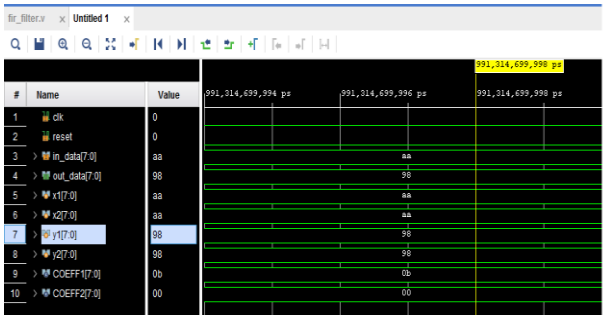

Fig8c. Simulation waveform for OBC DA Filter

Table. 1

S. No	FILTERS	POWER(W)	DELAY (ns)	LUT
1	DA	10.218	13.218	120
2	OBC DA	8.368	5.93	21

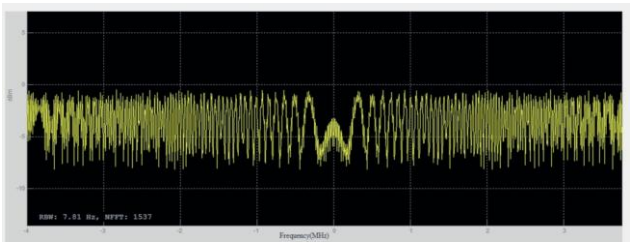

Fig9a. Input signal to the decimation filter

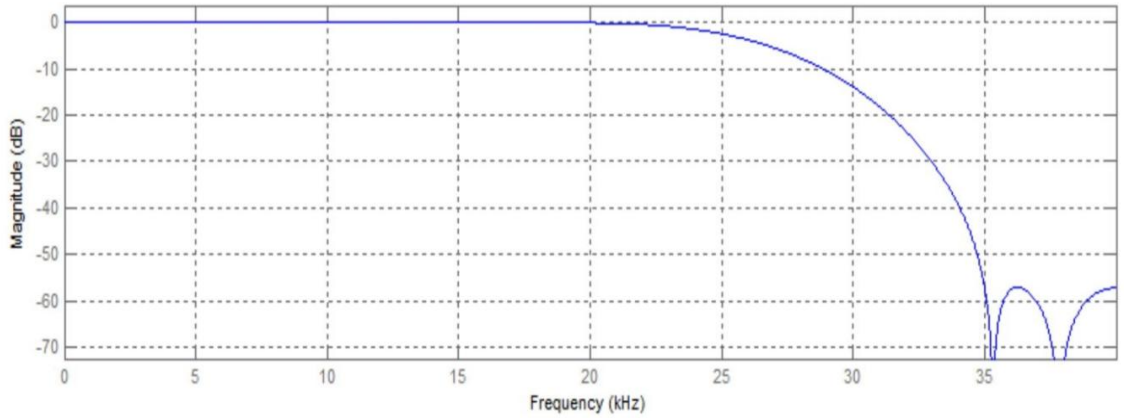

Fig9b. Frequency response of the corrector filter

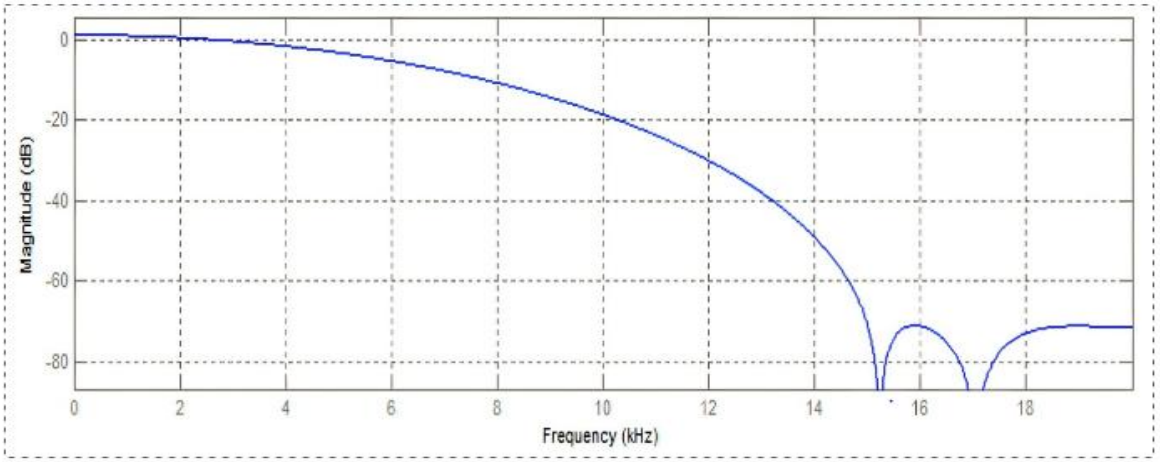

Fig9c. Frequency response of the corrector filter

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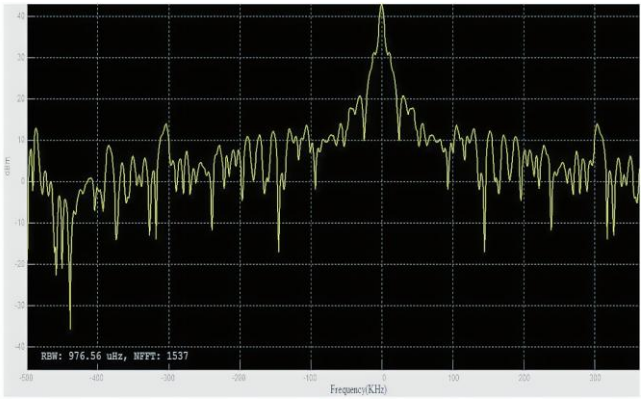

Fig 9d. Frequency response of the decimation filter

V. CONCLUSION

In this paper, a reconfigurable CSD-based FIR decimation filter has been proposed for digital hearing aid applications. The power is (mW), delay, and LUT reports for the FIR filter with eight taps have been presented. The Binary DA and OBC DA FIR filters occupy more area than the conventional FIR filter. The Binary DA architecture consumes more power due to its high LUT requirement and delay. On the other hand, the OBC DA architecture has a comparatively lower LUT requirement and less delay, resulting in increased speed. Moreover, the area of the OBC DA architecture is less than that of the DA architecture due to the reduction in ROM. Therefore, the OBC DA architecture is highly preferred over the DA architecture due to its lower power consumption, lower delay, and higher speed.

DECLARATION

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Conflicts of Interest/ Competing Interests	No conflicts of interest to the best of our knowledge.
Ethical Approval and Consent to Participate	No, the article does not require ethical approval or consent to participate, as it presents evidence.
Availability of Data and Material/ Data Access Statement	Yes, It is relevant.(ieeexplore.ieee.com) and (scholar.google.com)
Authors Contributions	I, K. Teja Sri, have completed this paperwork under the guidance of Dr. S. V. V. Satyanarayana, Assistant Professor at SVEC, Tadepalligudem.

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